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MODEL NAME : QXW00
PCB NO : LA-7901P (DA60000PM00)
BOM P/N : 4619F631L01 / L02
GPIO MAP: E4_VC_GPIO_map_rev_1.1

Korbel 14 UMA--Non vPRO
Ivy/Sandy Bridge + Panther POINT(HM77w/DASH)

2012-03-03


REV : 1.0 (A00)

@ : Nopop Component
CONN@ : Connector Component

| MB Type | BOM P/N | |
|---------------|---------|----------|
| TPM | 43* | 1@ 3@ 5@ |
| TCM | | 2@ 4@ 5@ |
| TPM DIS | | 2@ 3@ |
| HM77 w/o Vpro | | |
| QM77 w/ Vpro | | |
| PCH XDP | | PXDP@ |
| HDMI LOGO | | 46@ |

| MB PCB | |
|-------------|-------------------------------|
| Part Number | Description |
| DA60000PM00 | PCB 0LH LA-7901P REV0 M/S UMA |

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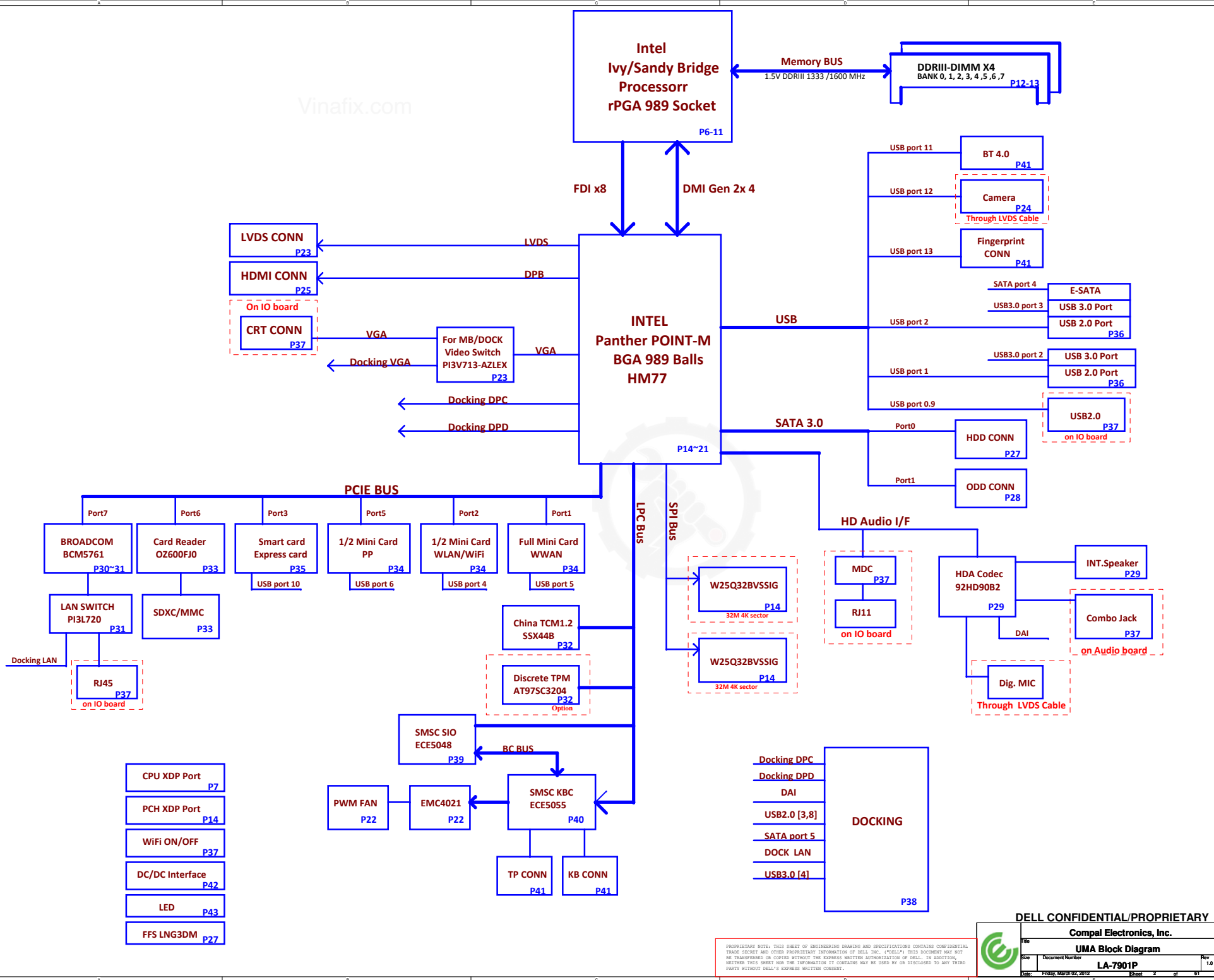
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Cover Sheet

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UMA Block Diagram

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POWER STATES

| Signal State | SLP S3# | SLP S4# | SLP S5# | SLP A# | ALWAYS PLANE | M PLANE | SUS PLANE | RUN PLANE | CLOCKS |
|------------------------------|------------|------------|------------|-----------|-----------------|------------|--------------|--------------|--------|
| S0 (Full ON) / M0 | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | ON | ON |
| S3 (Suspend to RAM) / M3 | LOW | HIGH | HIGH | HIGH | ON | ON | ON | OFF | OFF |
| S4 (Suspend to DISK) / M3 | LOW | LOW | HIGH | HIGH | ON | ON | OFF | OFF | OFF |
| S5 (SOFT OFF) / M3 | LOW | LOW | LOW | HIGH | ON | ON | OFF | OFF | OFF |
| S3 (Suspend to RAM) / M-OFF | LOW | HIGH | HIGH | LOW | ON | OFF | ON | OFF | OFF |
| S4 (Suspend to DISK) / M-OFF | LOW | LOW | HIGH | LOW | ON | OFF | OFF | OFF | OFF |
| S5 (SOFT OFF) / M-OFF | LOW | LOW | LOW | LOW | ON | OFF | OFF | OFF | OFF |

PM TABLE

| power plane State | +15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO | +3.3V_SUS +1.5V_MEM | +5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN | +3.3V_M +1.05V_M | +3.3V_M +1.05V_M (M-OFF) |
|-------------------------|---|------------------------|---|---------------------|--------------------------------|
| S0 | ON | ON | ON | ON | ON |
| S3 | ON | ON | OFF | ON | OFF |
| S5 S4/AC | ON | OFF | OFF | ON | OFF |
| S5 S4/AC don't exist | OFF | OFF | OFF | OFF | OFF |

need to update Power Status and
PM Table

| USB 3.0 PORT# | Connetion |
|---------------|-------------------|
| 1 | NA |
| 2 | JUSB1 (Left side) |
| 3 | JUSB2 (Left side) |
| 4 | DOCKING |

| PCH | USB PORT# | DESTINATION |
|-----|-----------|---------------------------|
| | 0 | JUSB (Right side-IO/B) |
| | 1 | JUSB (Left side) |
| | 2 | JESA1 (Leftt side ESATA) |
| | 3 | MLK DOCK |
| | 4 | WLAN |
| | 5 | WWAN |
| | *1 6 | JMINI3(Flash)-for w/ Vpro |
| | *1 7 | DOCKING |
| | 8 | NA |
| | 9 | JUSB (Right side-Audio/B) |
| | 10 | Express card/Smart Card |
| | 11 | Bluetooth |
| | 12 | Camera |
| | 13 | BIO |

*1: HM76 don't support port 6,7

| SATA | DESTINATION |
|--------|--------------------|
| SATA 0 | HDD |
| SATA 1 | ODD/ E3 Module Bay |
| SATA 2 | NA |
| SATA 3 | NA |
| SATA 4 | ESATA |
| SATA 5 | Dock |

| UMA DP/HDMI Port | Connetion |
|------------------|----------------|
| Port B | MB HDMI Conn |
| Port C | Dock DP port 2 |
| Port D | Dock DP port 1 |

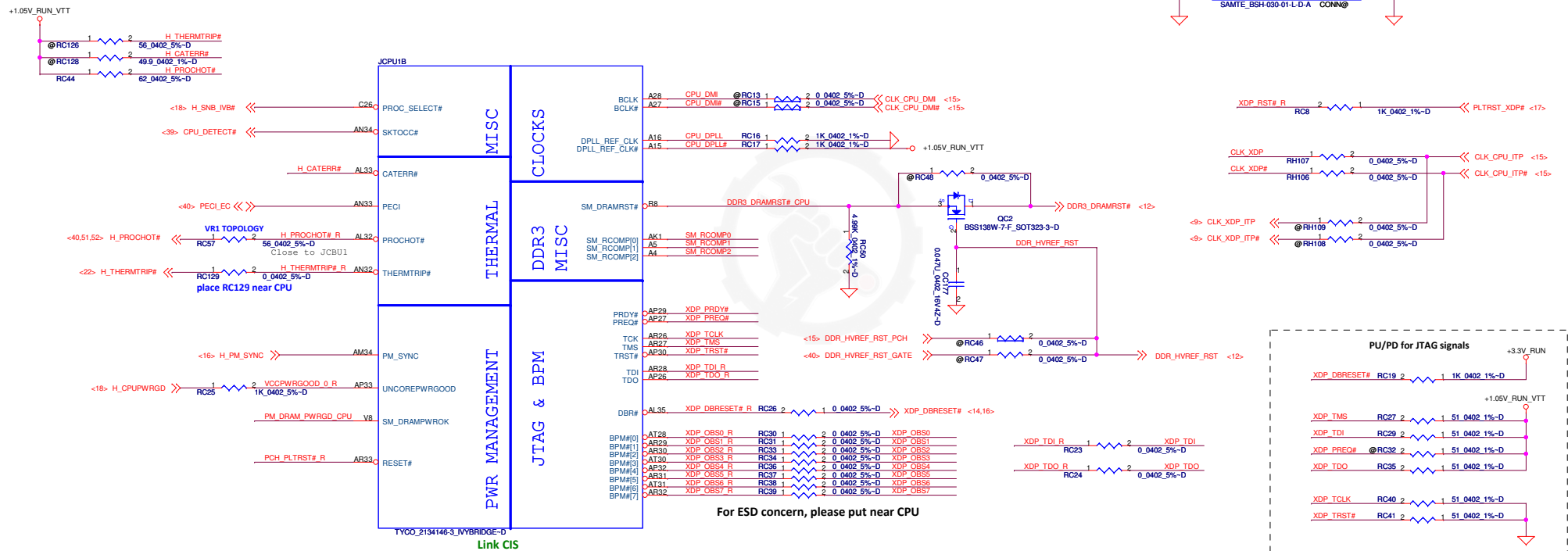
| PCI EXPRESS | DESTINATION |
|-------------|----------------------|
| Lane 1 | MINI CARD-1 WWAN |
| Lane 2 | MINI CARD-2 WLAN |
| Lane 3 | Express card |
| Lane 4 | None |
| Lane 5 | 1/2vMINI CARD-3 PCIE |
| Lane 6 | MMI |
| Lane 7 | 10/100/1G LOM |
| Lane 8 | None |

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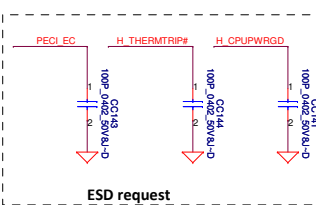
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| Index and Config. | | | |
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Follow DG Rev0.71 SM_DRAMPWROK topology

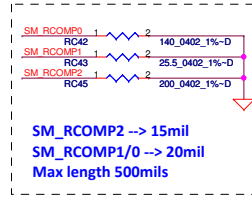


The schematic diagram illustrates an open drain buffer circuit. The input signal, labeled <14.17> PCH_PLTRST#, is connected to the input of the UC1 buffer IC. The output of the buffer is labeled PCH_PLTRST#_B. The circuit is powered by +3.3V_RUN and +1.05V_RUN_VTT. A 0.1uF capacitor is connected between the output of the buffer and the +3.3V_RUN supply. A 75 ohm resistor is connected between the output of the buffer and the +1.05V_RUN_VTT supply. A 43.0402 5% D resistor is connected between the output of the buffer and ground. The UC1 buffer IC is identified as SN74VCT07DCKR_SCT05-D.



Place closed JCPU
XDP_DBRESET#

Avoid stub in the PWRGD path while placing resistors RC25 & RC130

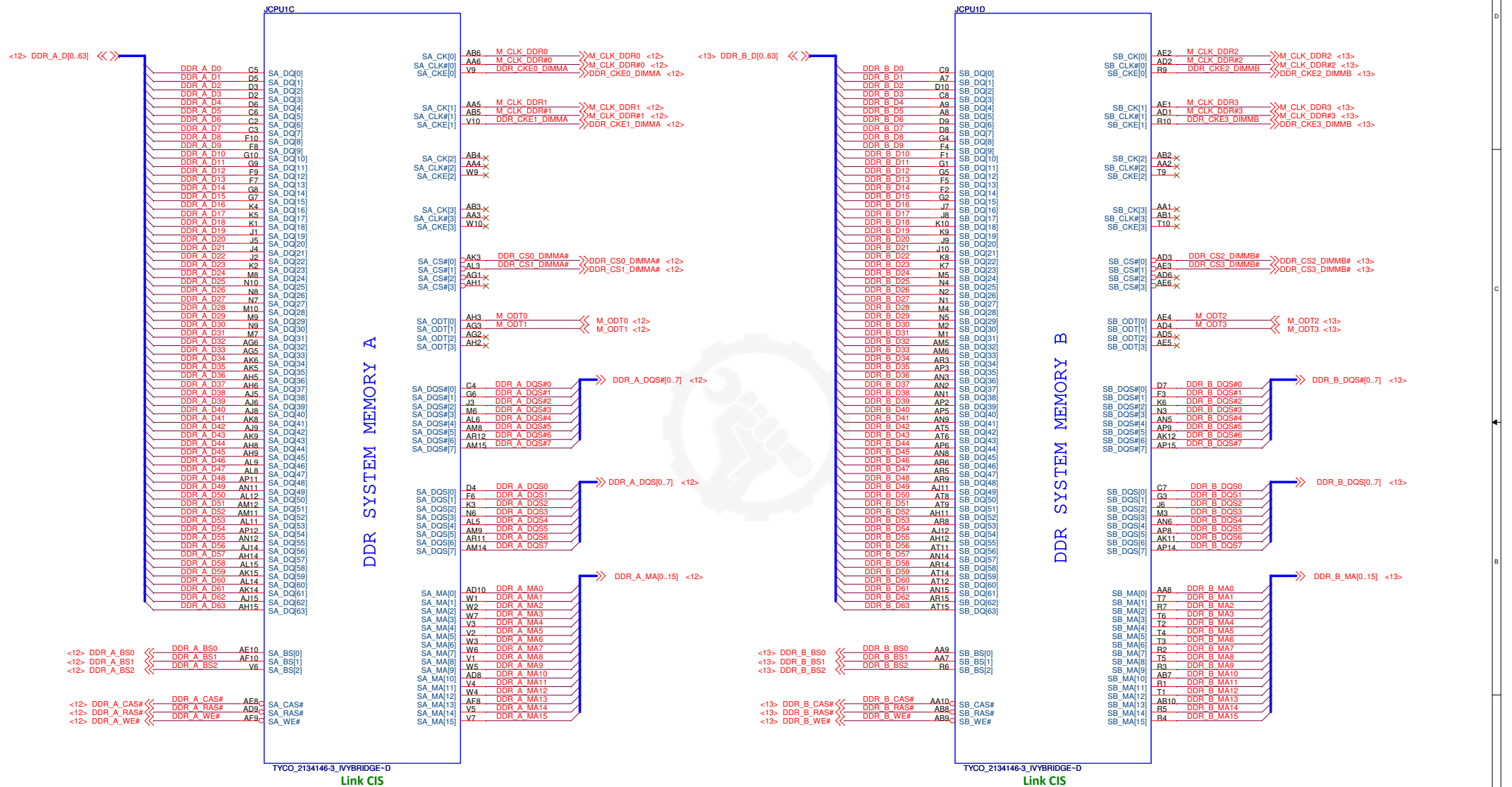


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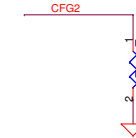
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CFG Straps for Processor



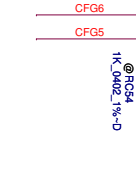
PEG Static Lane Reversal - CFG2 is for the 16x

| CFG2 | 1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed |
|------|---|
|------|---|



Display Port Presence Strap

| CFG4 | 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port |
|------|--|
|------|--|



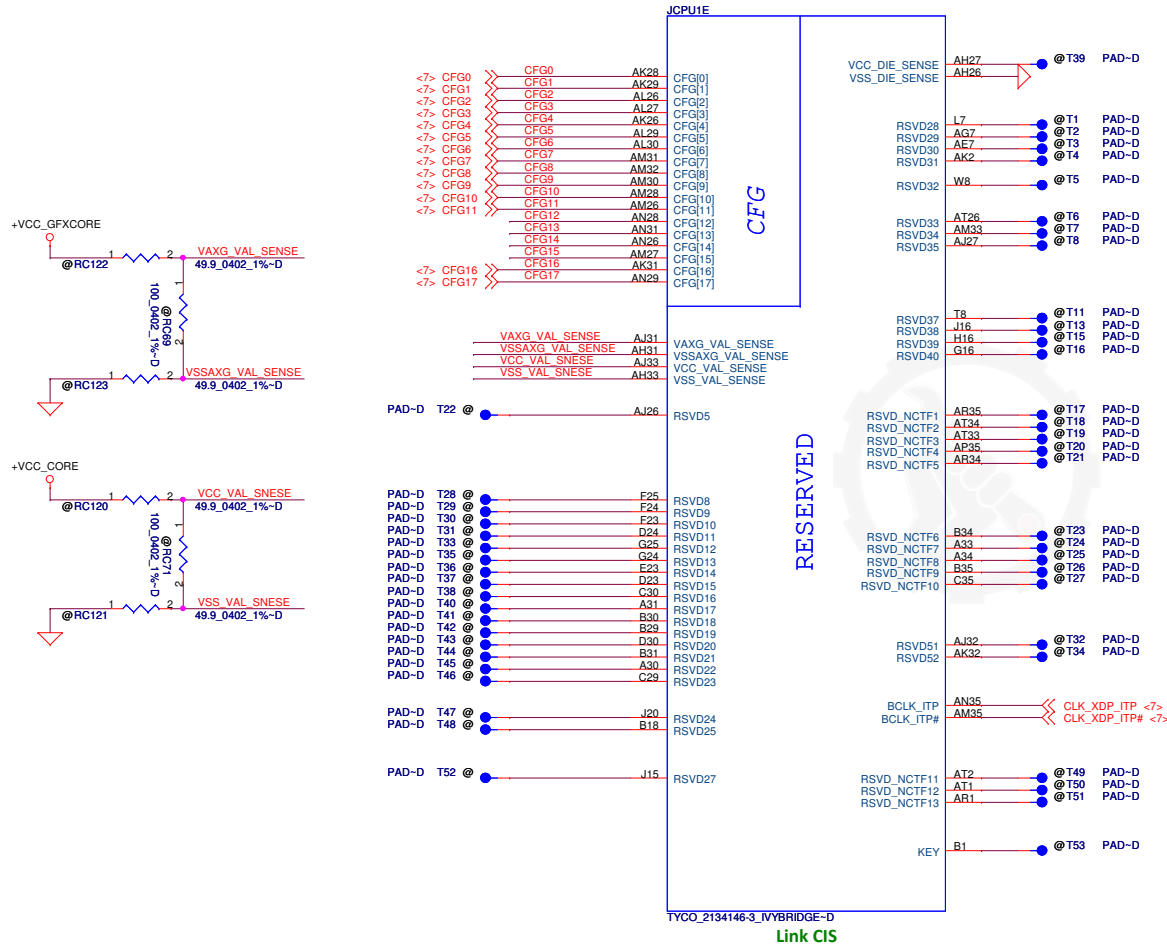
PCIe Port Bifurcation Straps

| CFG[6:5] | 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled |
|----------|--|
|----------|--|



PEG DEFER TRAINING

| CFG7 | 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training |
|------|---|
|------|---|



TYCO_2134146-3_IVYBRIDGE-D

Link CIS



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Ivy/Sandy Bridge (4/6)

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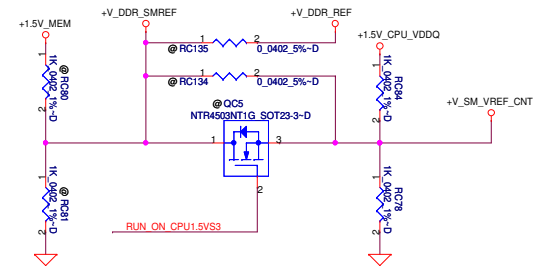
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3.1.5V_CPU_VDDQ Source

The schematic diagram illustrates the 1.5V_CPU_VDDQ power source circuit. It features a 3.3V_ALW2 input connected to a network of resistors (RC72, RC74) and a capacitor (C72). This network drives the gate of an NMOS transistor (Q7A). The source of Q7A is grounded, and its drain provides the 1.5V_CPU_VDDQ output. The output is connected to a 20k resistor (RC73) and a capacitor (C73). A 1M resistor (RC43) and a capacitor (C78) connect the 1.5V_CPU_VDDQ output to the 1.5V_MEM input. The 1.5V_MEM input is connected to the gate of a PMOS transistor (Q7B). The source of Q7B is connected to the 1.5V_CPU_VDDQ output, and its drain is connected to the 1.5V_CPU_VDDQ input. The 1.5V_CPU_VDDQ input is connected to the 1.5V_MEM input through a 1M resistor (RC43) and a capacitor (C78).



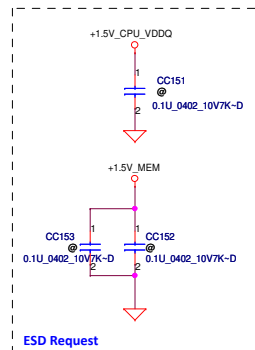
POWER

GRAPHICS

MISC

ESD Request

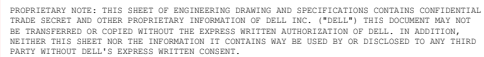
Depoc RC140 for ES2 CPU

[illegible]

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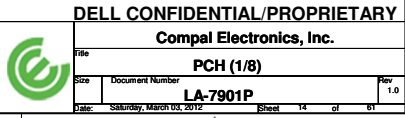


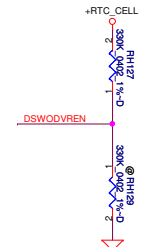
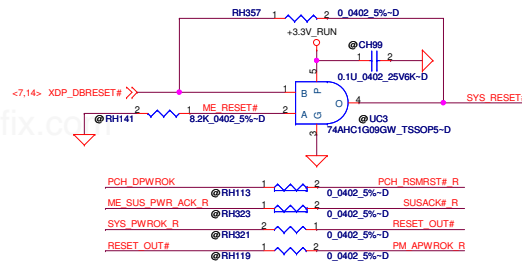
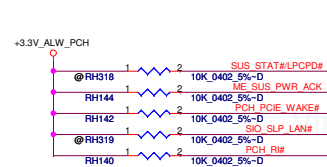




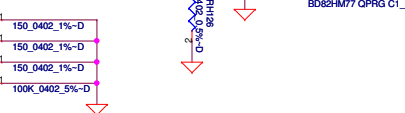
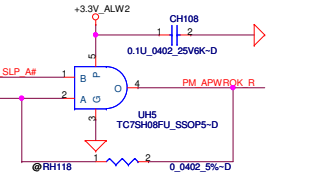
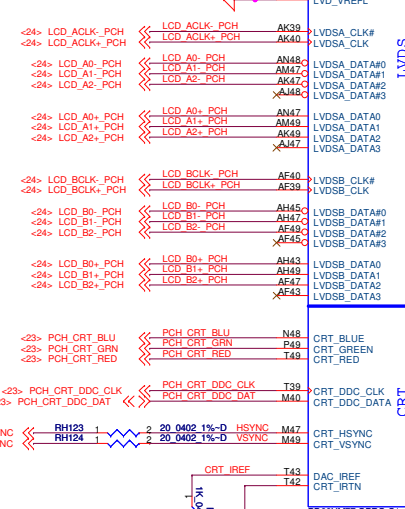
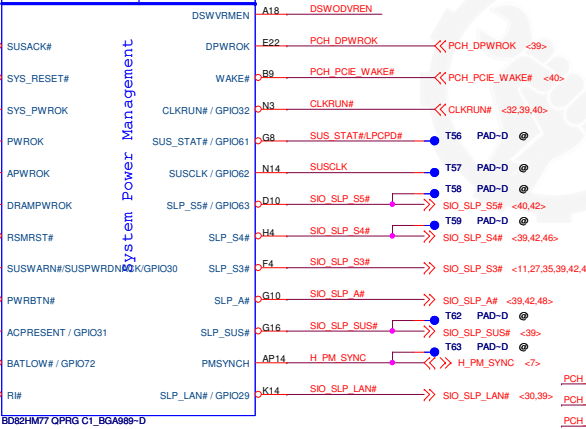
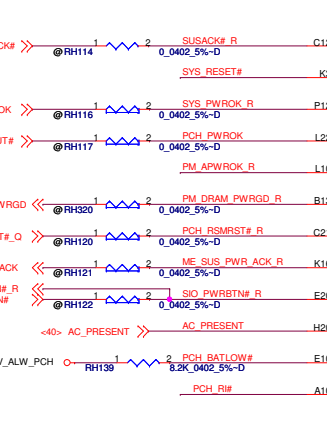
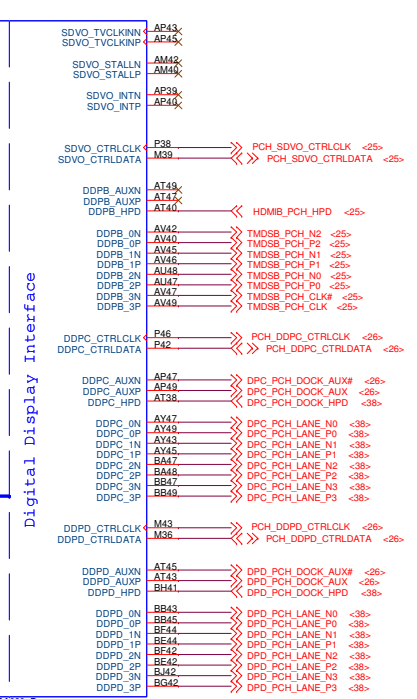
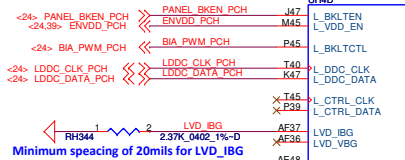
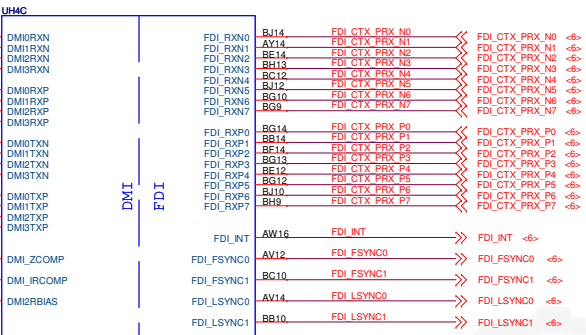
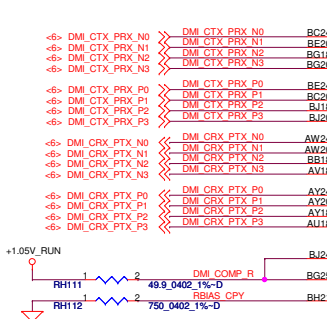
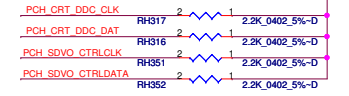
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| DSWODVREN - On Die DSW VR Enable | |
|----------------------------------|---|
| Enabled (DEFAULT) | HIGH: RH127 STUFFED, RH129 UNSTUFFED |
| Disabled | LOW: RH129 STUFFED, RH127 UNSTUFFED |



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PCH (3/8)

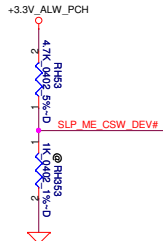
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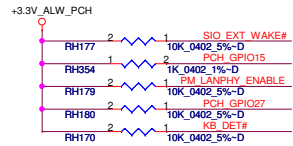


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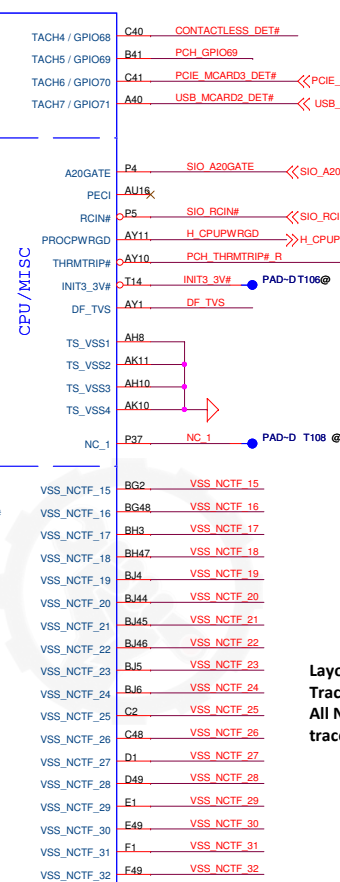
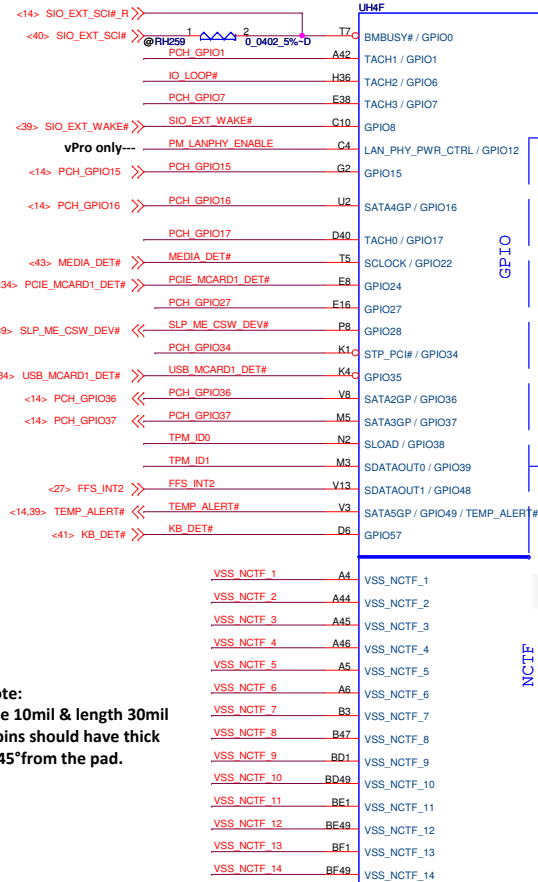


Note: PCH has internal pull up 20k ohm on E3_PAID_TS_DET# (GPIO27)

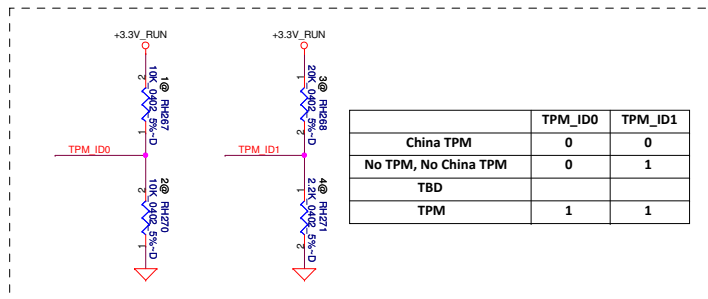
| SLP_ME_CSW_DEV# PLL ON DIE VR ENABLE | |
|--------------------------------------|----------------|
| ENABLED | HIGH (DEFAULT) |
| DISABLED | LOW |



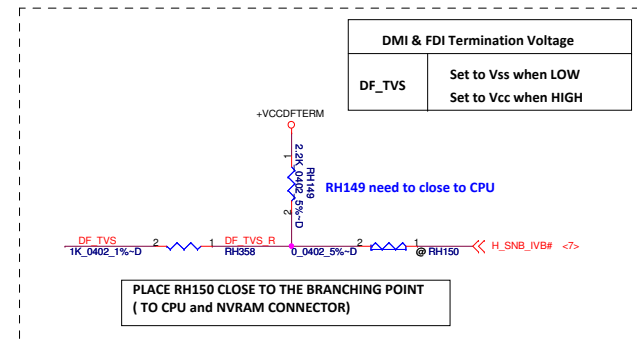
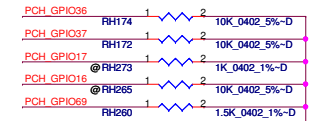
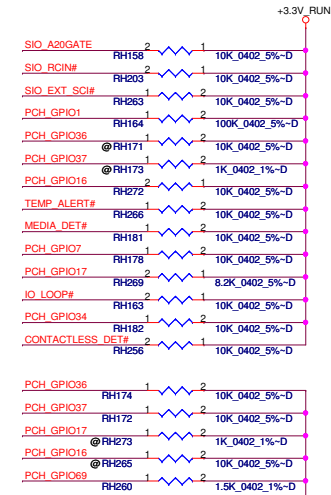
Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45° from the pad.



Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45° from the pad.



| | TPM_ID0 | TPM_ID1 |
|----------------------|---------|---------|
| China TPM | 0 | 0 |
| No TPM, No China TPM | 0 | 1 |
| TBD | | |
| TPM | 1 | 1 |



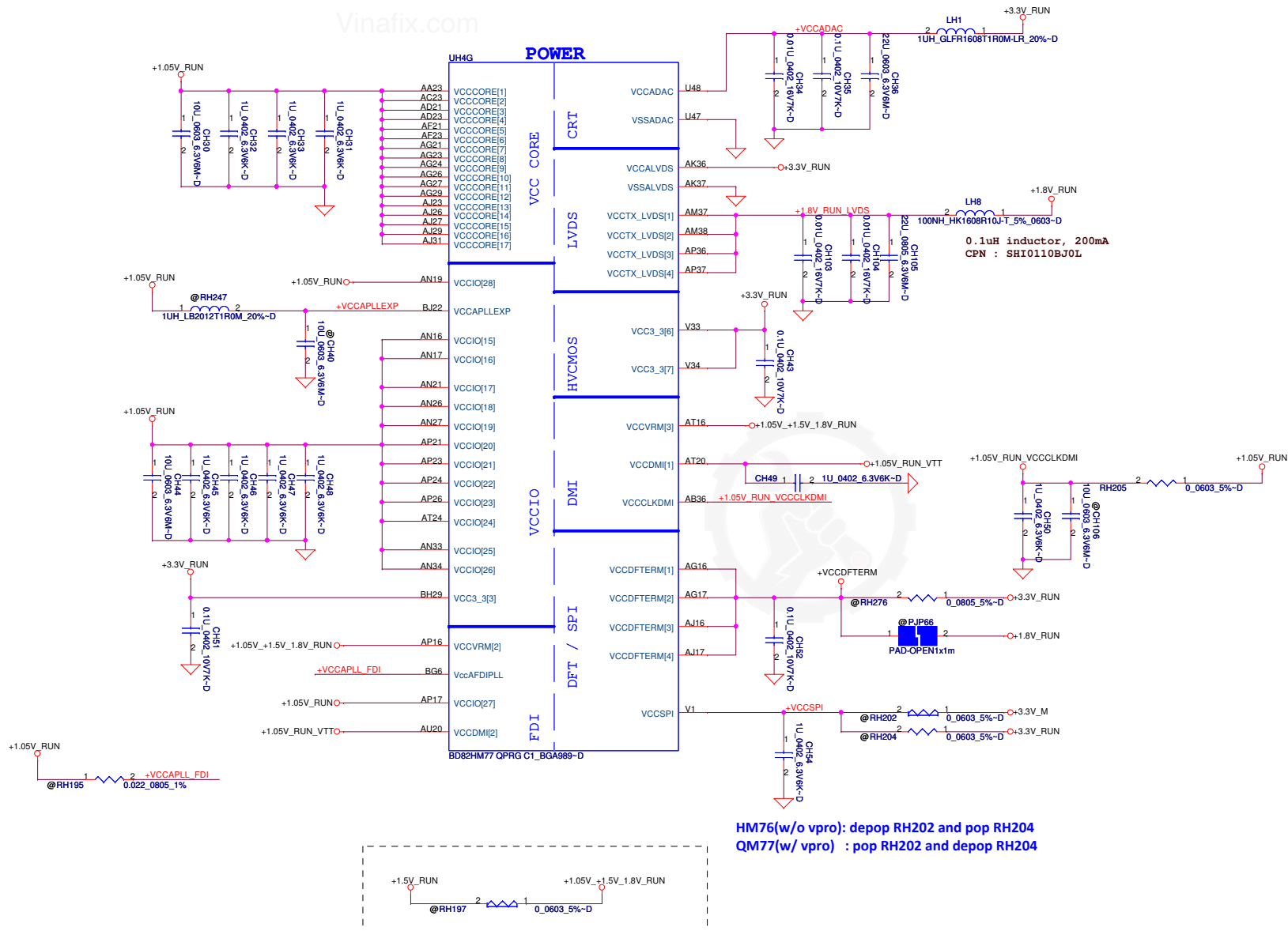
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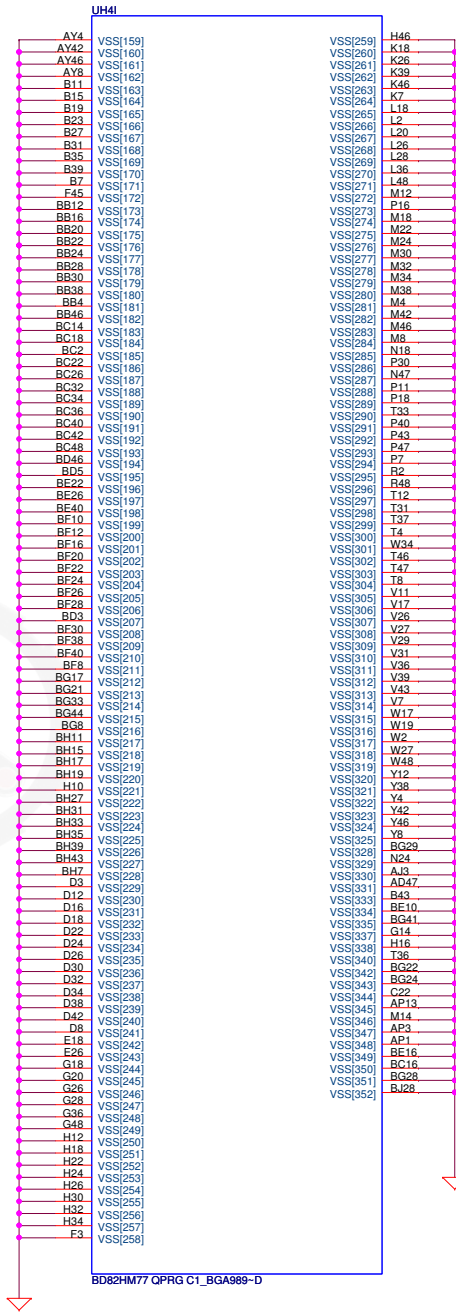
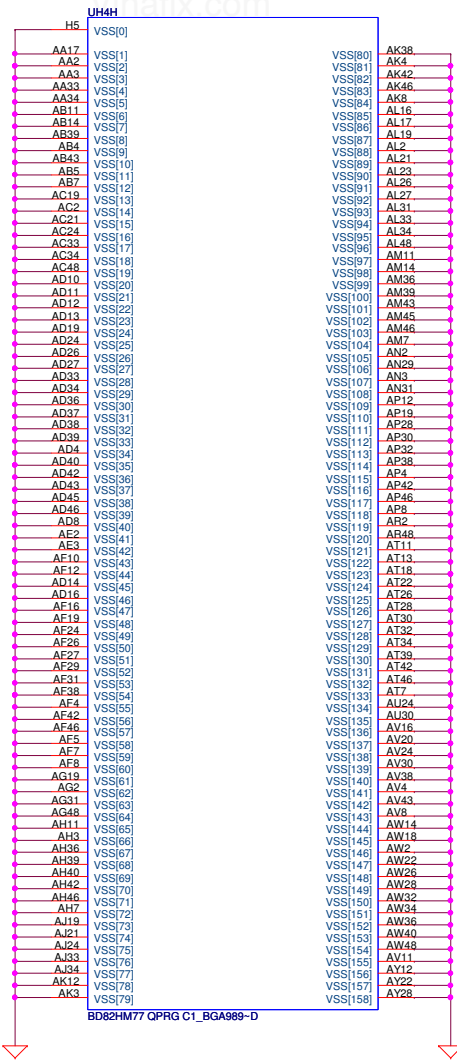
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HM76(w/o vpro): depop RH202 and pop RH204
QM77(w/ vpro) : pop RH202 and depop RH204

| PCH Power Rail Table | | |
|----------------------|-----------|-----------------------|
| Voltage Rail | Voltage | SO Iccmax Current (A) |
| V_PROC_IO | 1.05 | 0.001 |
| V5REF | 5 | 0.001 |
| V5REF_Sus | 5 | 0.001 |
| Vcc3_3 | 3.3 | 0.288 |
| VccADAC3 | 3.3 | 0.063 |
| VccADPLLA | 1.05 | 0.08 |
| VccADPLLB | 1.05 | 0.08 |
| VccCore | 1.05 | 1.7 |
| VccDMI | 1.05 | 0.047 |
| VccIO | 1.05 | 3.711 |
| VccASW | 1.05 | 0.903 |
| VccSPI | 3.3 | 0.01 |
| VccDSW3_3 | 3.3 | 0.001 |
| VCCDFTerm | 1.8 | 0.002 |
| VccRTC | 3.3 | 6uA |
| VccSus3_3 | 3.3 | 0.126 |
| VccSusHDA | 3.3 | 0.01 |
| VccVRM | 1.8 / 1.5 | 0.167 |
| VccClkDMI | 1.05 | 0.07 |
| VccSSC | 1.05 | 0.095 |
| VccDIFFCLKN | 1.05 | 0.055 |
| VccALVDS | 3.3 | 0.001 |
| VccTX_LVDS | 1.8 | 0.04 |
| | | |
| | | |
| | | |



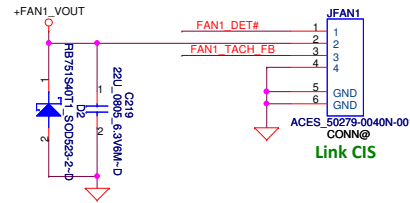
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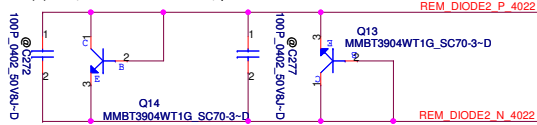
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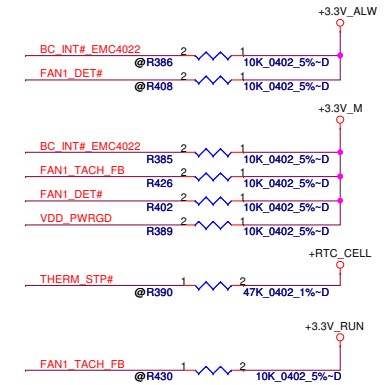
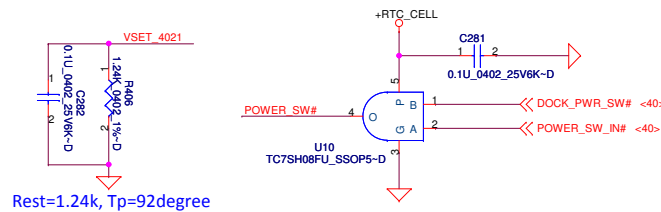
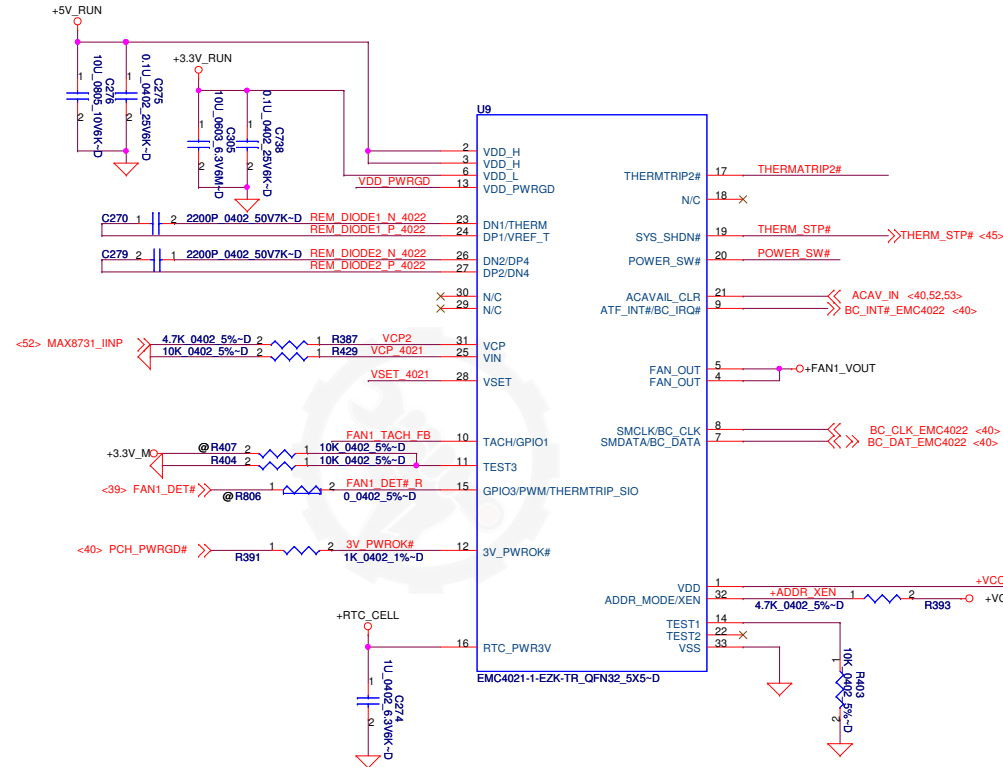
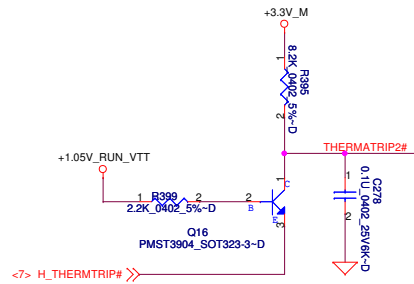


HM76(w/o vpro): depop R385 and pop R386
QM77(w/ vpro) : pop R385 and depop R386

- (1) DP3/DN3 for SODIMM on Q14, place Q14 close to SODIMM and C272 close to Q14
- (2) DP5/DN5 for Skin on Q13, place Q13 close to Vcore VR choke.



Place under CPU
Place C266 close to the Q12 as possible



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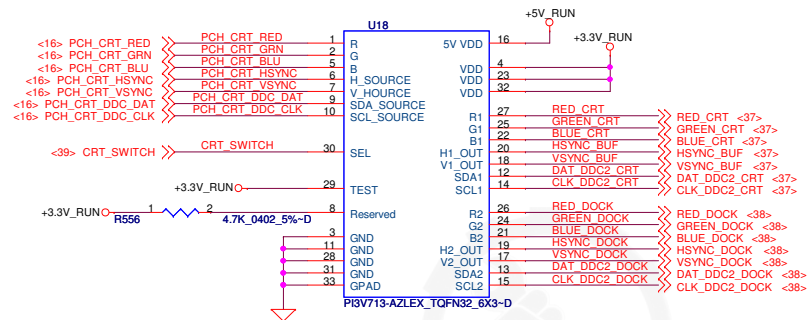
Compal Electronics, Inc.

| FAN & Thermal Sensor | | | |
|------------------------------|-----------------|-----|-----|
| Title | Document Number | Rev | 1.0 |
| Size | LA-7901P | | |
| Date: Friday, March 02, 2012 | Sheet 22 | of | 61 |

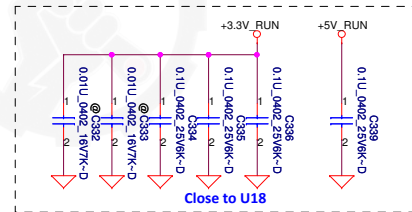
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SW for MB/DOCK



| SEL1/SEL2 | Chanel | Source |
|-----------|--------|---------|
| 0 | A=B1 | MB |
| 1 | A=B2 | APR/SPR |



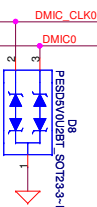
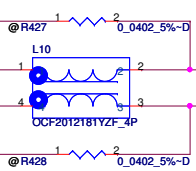
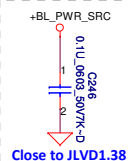
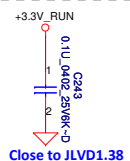
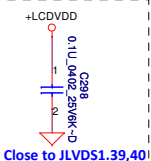
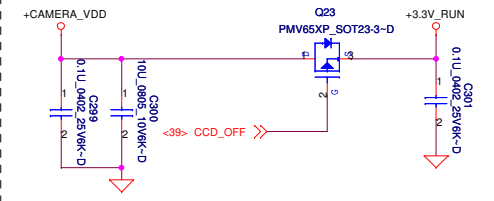
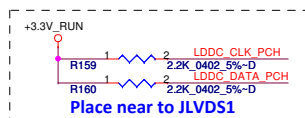
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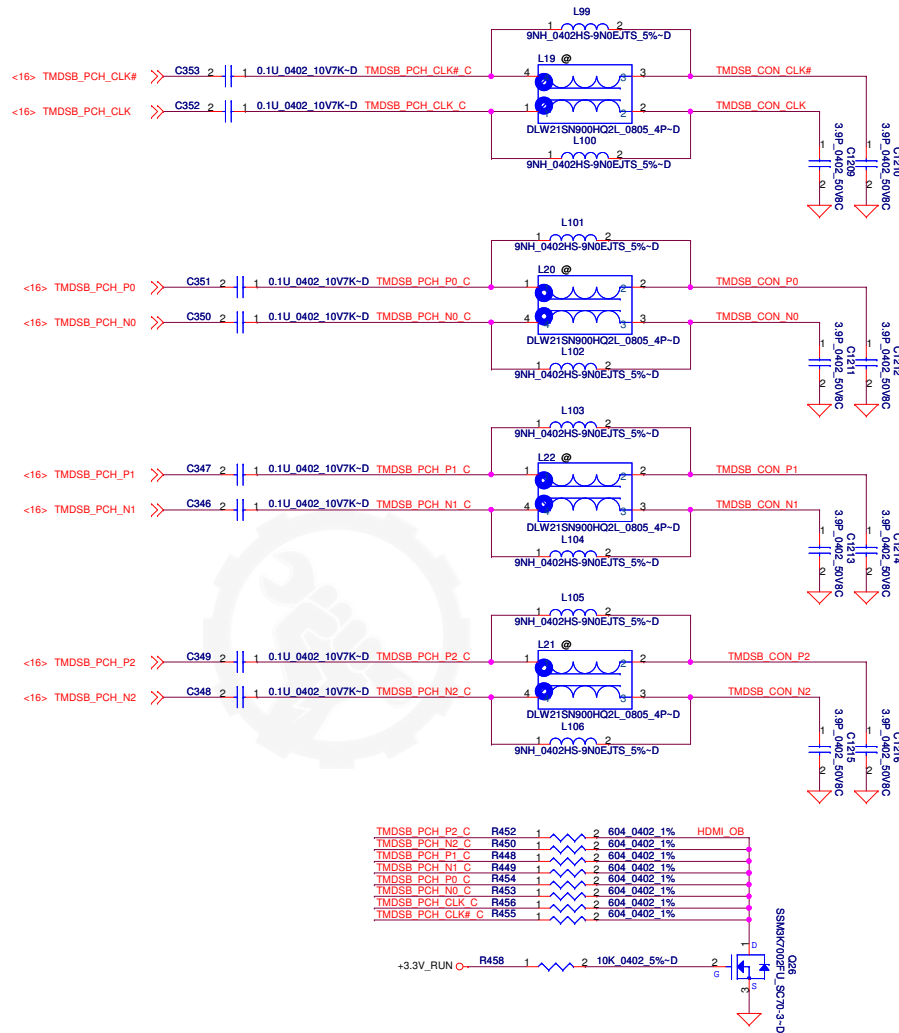


| Title | | |
|------------------|------------------------|----------------|
| CRT/Video switch | | |
| Size | Document Number | Rev |
| | LA-7901P | 1.0 |
| Date: | Friday, March 02, 2012 | Sheet 23 of 61 |

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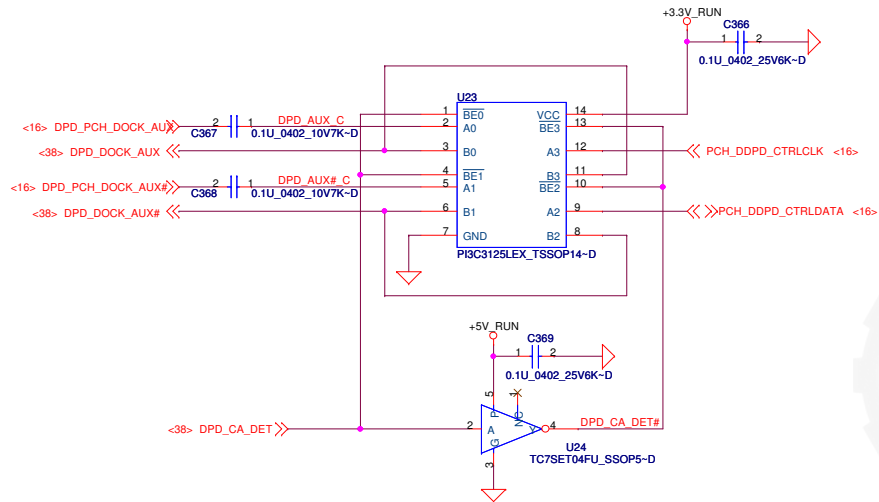
[illegible]

| Signal | Pin | Value | Unit | Frequency | Power | Notes |
|------------------|------|-------|------|-----------|---------|---------|
| TMDSB_PCH_P2_C | R452 | 1 | 2 | 604 | 0402 1% | HDMI OE |
| TMDSB_PCH_N2_C | R450 | 1 | 2 | 604 | 0402 1% | |
| TMDSB_PCH_P1_C | R448 | 1 | 2 | 604 | 0402 1% | |
| TMDSB_PCH_N1_C | R449 | 1 | 2 | 604 | 0402 1% | |
| TMDSB_PCH_P0_C | R454 | 1 | 2 | 604 | 0402 1% | |
| TMDSB_PCH_N0_C | R453 | 1 | 2 | 604 | 0402 1% | |
| TMDSB_PCH_CLK_C | R456 | 1 | 2 | 604 | 0402 1% | |
| TMDSB_PCH_CLK#_C | R455 | 1 | 2 | 604 | 0402 1% | |

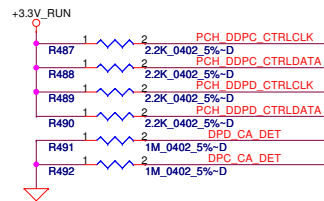
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|--------------------------------------|--------------------------|-------|------------|
| DELL CONFIDENTIAL/PROPRIETARY | | | |
| Compal Electronics, Inc. | | | |
| Title | | | |
| HDMI port | | | |
| Size | Document Number | | Rev |
| | LA-7901P | | 1.0 |
| Date: | Saturday, March 03, 2012 | Sheet | 25 of 61 |

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AUX/DDC SW for DPD to E-DOCK



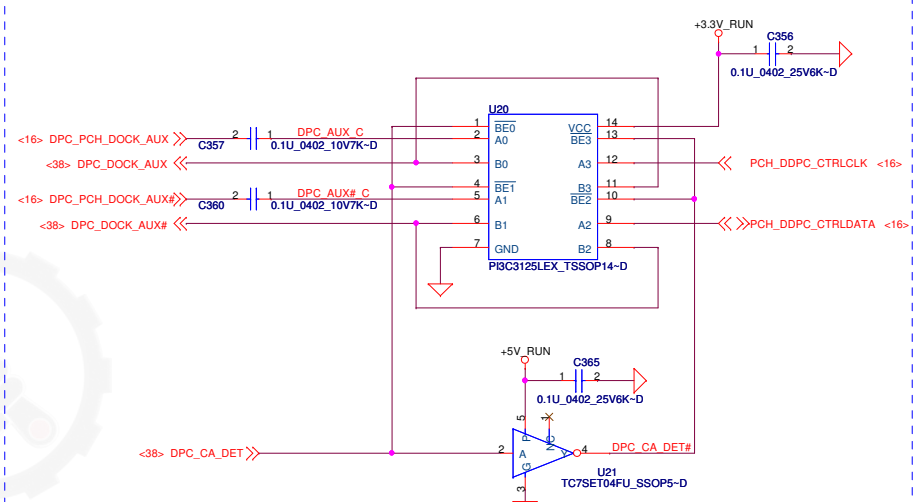
Note:When implement 2nd source, please check Vil and Vih spec is meet main source spec



Intel WW18 Strapping option

Intel WW18 Strapping option

AUX/DDC SW for DPC to E-DOCK



Note:When implement 2nd source, please check Vil and Vih spec is meet main source spec

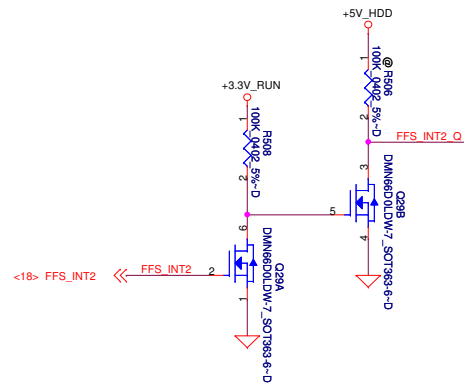
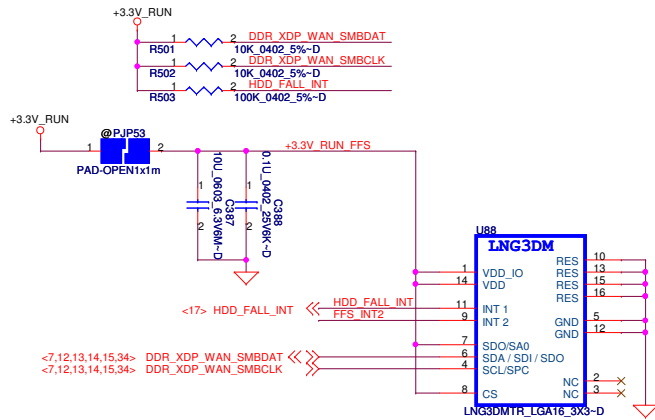
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Compal Electronics, Inc.

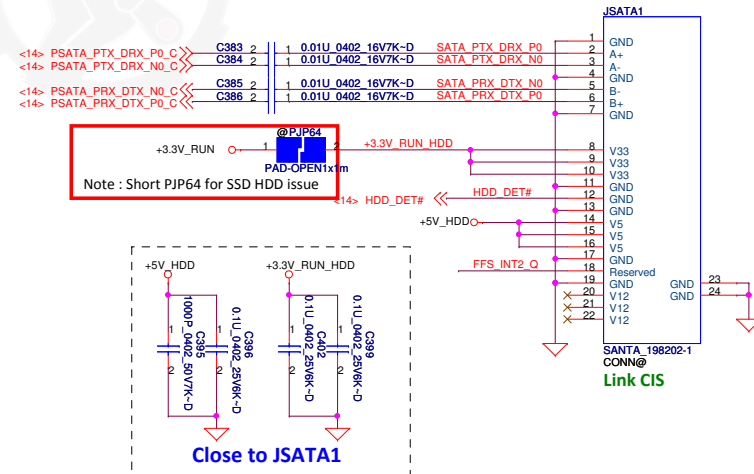
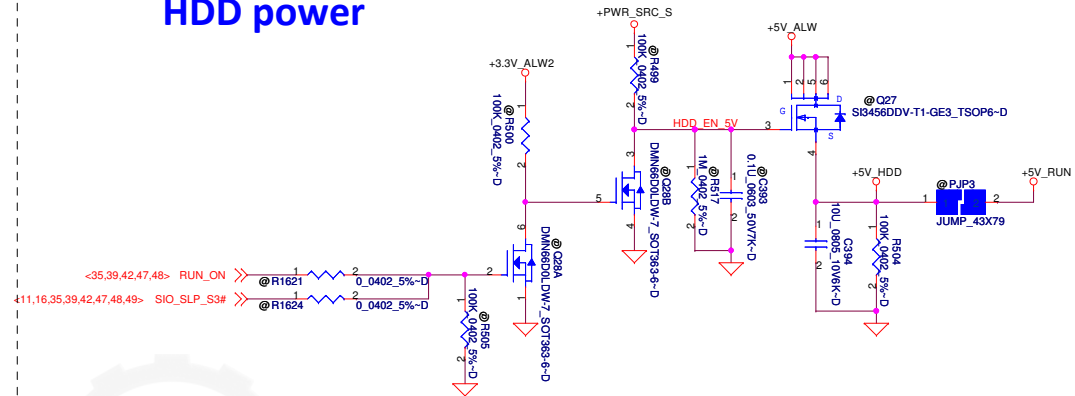


| Title | | |
|-------|------------------------|----------------|
| DP SW | | |
| Size | Document Number | Rev |
| | LA-7901P | 1.0 |
| Date: | Friday, March 02, 2012 | Sheet 26 of 61 |

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HDD power



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HDD CONNECTOR

LA-7901P

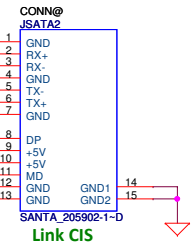
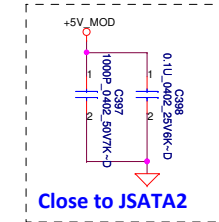
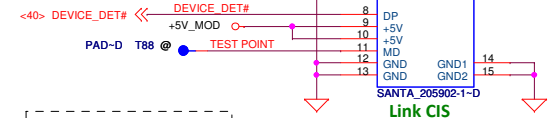
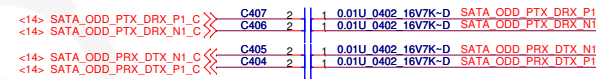
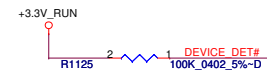
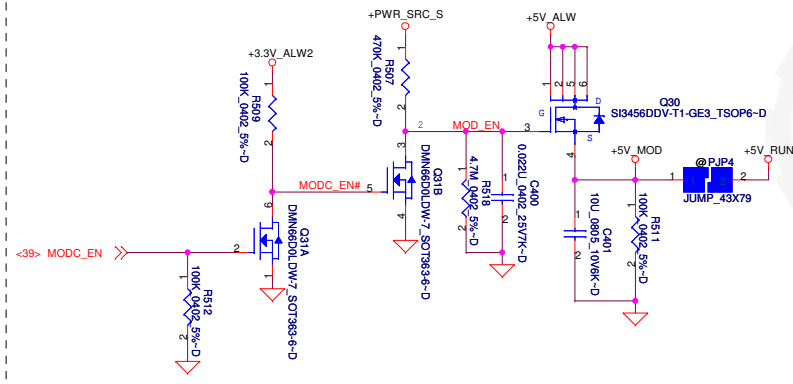
Rev 1.0

Date: Friday, March 02, 2012

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ODD power

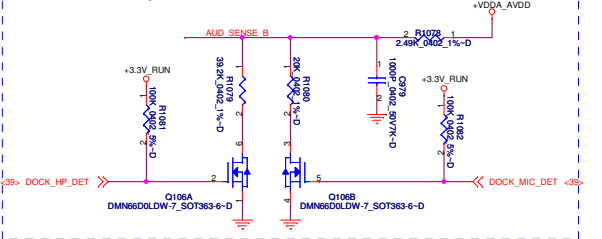
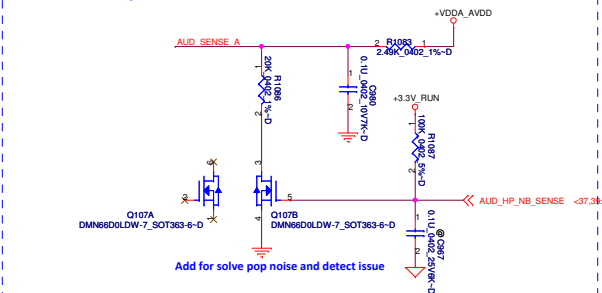
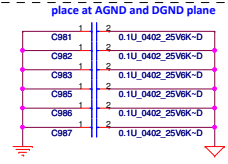
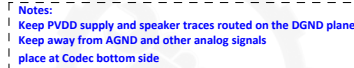
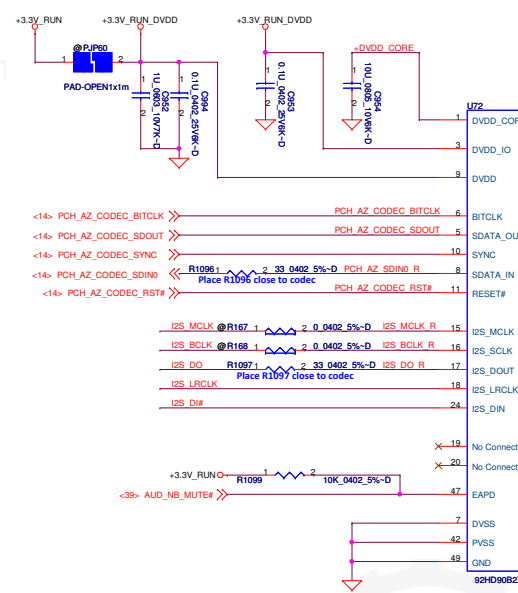


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| Title | | | |
|---------------|------------------------|-------|----------|
| ODD CONNECTOR | | | |
| LA-7901P | | | |
| Date: | Friday, March 02, 2012 | Sheet | 28 of 61 |

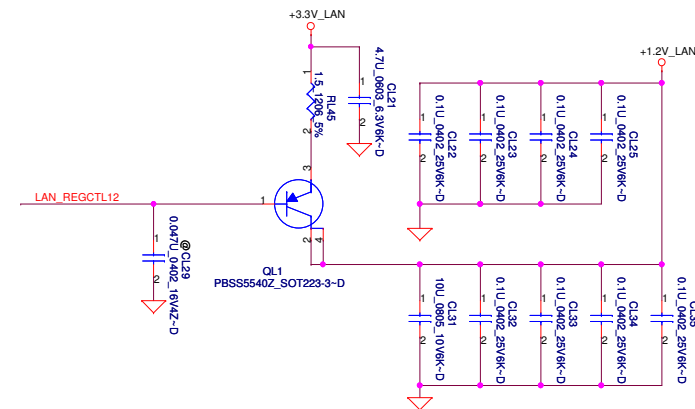
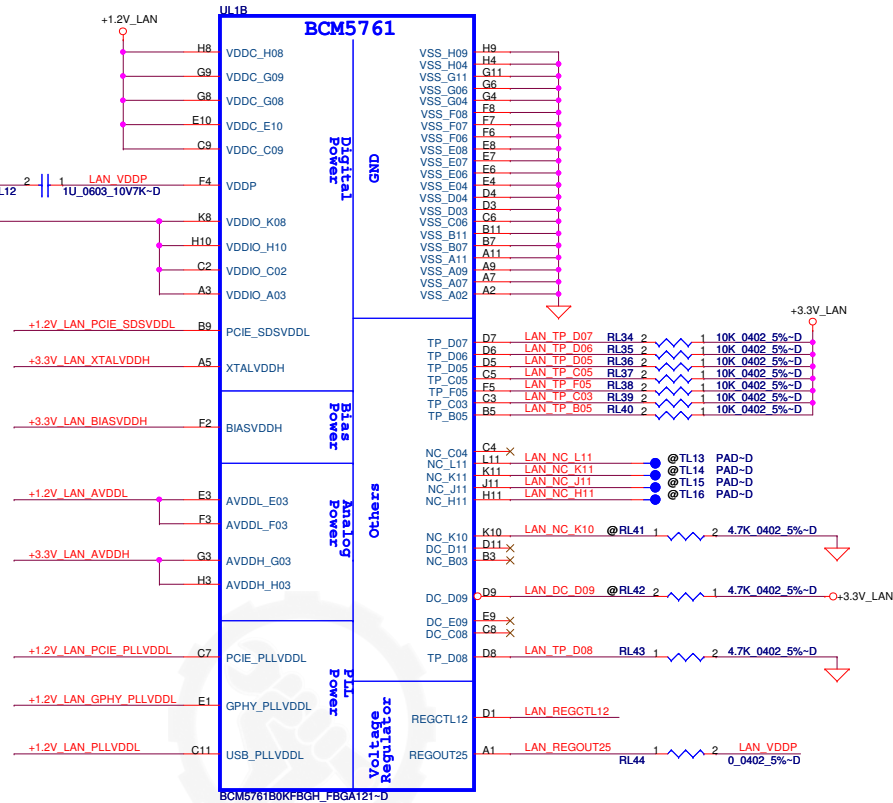
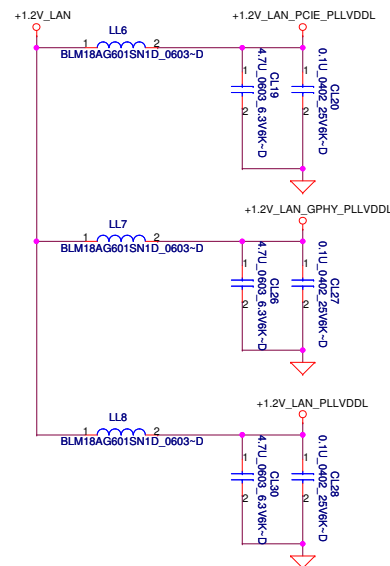
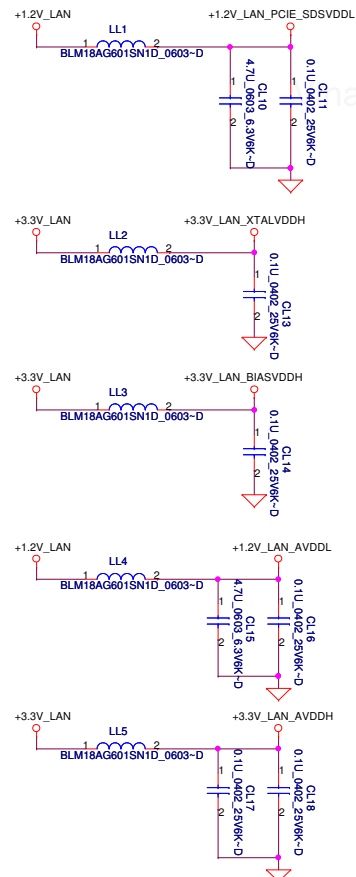
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[illegible]

| Resistor | SENSE_A | SENSE_B |
|----------|-----------------|-------------------|
| 39.2K | PORT A | PORT E |
| 20K | PORT B | PORT F |
| 10K | NA | DMIC0 |
| 5.11K | SPDIFOUT0 | SPDIFOUT1 (DMIC1) |
| 2.49K | Pull-up to AVDD | |

[illegible]

| | | |
|--------------------------|-----------------|------------|
| Title | | |
| Azalia (HD) Codec | | |
| Size | Document Number | Rev |
| | LA-7901P | 1.0 |

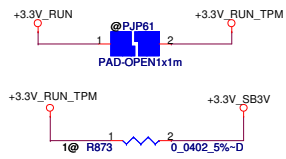


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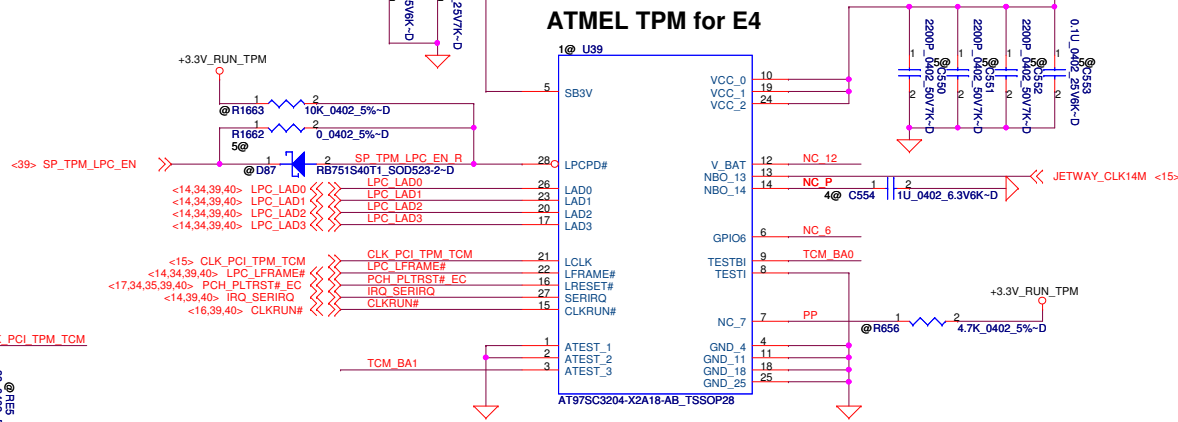


| | | | |
|--------------------------|--|--|--|
| Compal Electronics, Inc. | | | |
| Title | | | |
| LAN (2/2) BCM5761 | | | |
| Size | | | |
| Document Number | | | |
| LA-7901P | | | |
| Date | | | |
| Friday, March 02, 2012 | | | |
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Vinafix.com

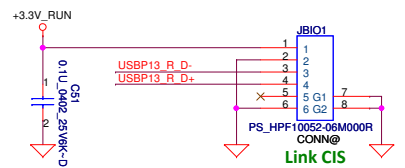
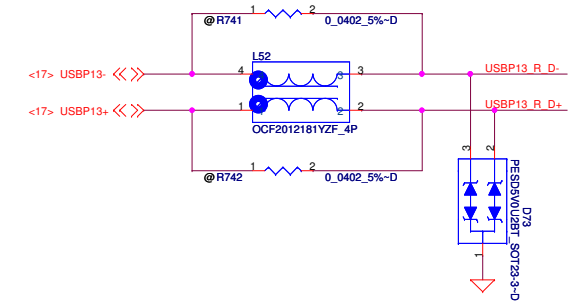
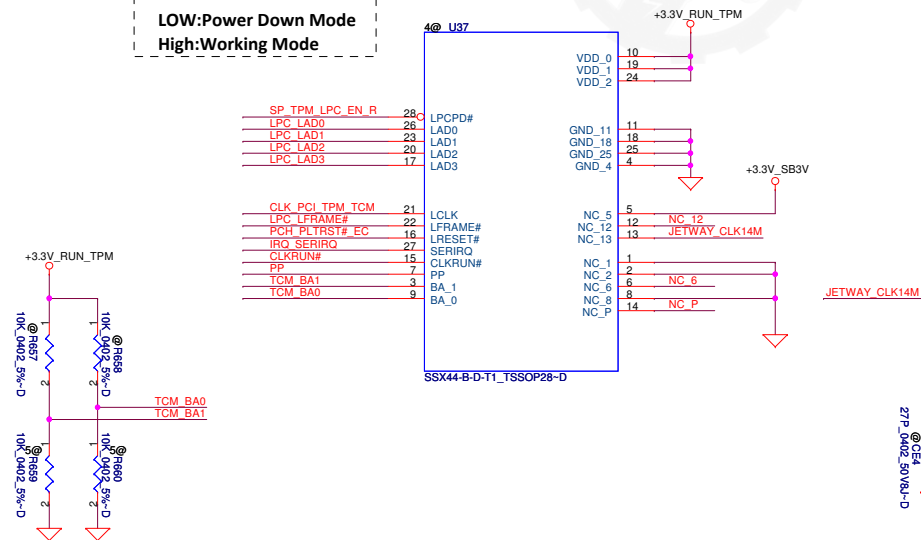


Co-lay U37 and U39

LPC layout: Place TCM first and then end LPC with TPM.

China TCM: NationZ & Jetway co-lay

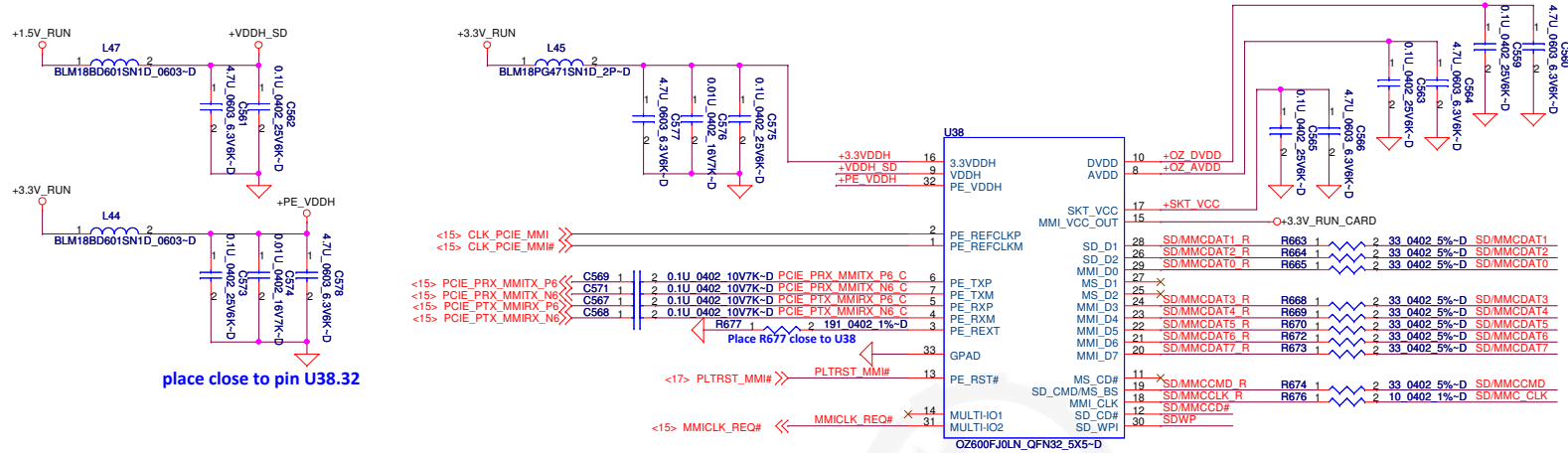
LOW:Power Down Mode
High:Working Mode



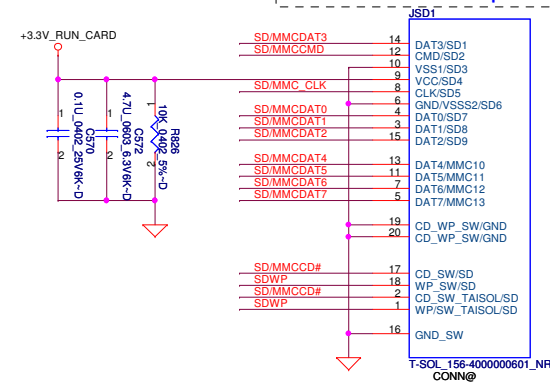
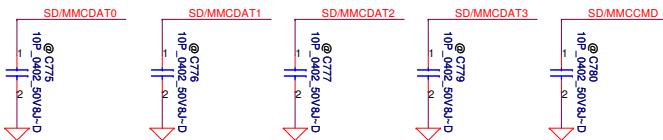
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| | | | |
|---|-----------------|---------------------------------|-------|
|  | | Compal Electronics, Inc. | |
| TPM/TCM/BIO Conn | | | |
| Size | Document Number | Rev 1.0 | |
| Date: Friday, March 02, 2012 | | Sheet 32 | of 61 |

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Vendor review in 6/22 and reserve for SD3.0 UHS-I 200MHz transfer



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Card Reader OZ600FJ0

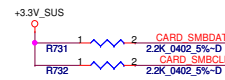
LA-7901P

Date: Friday, March 02, 2012

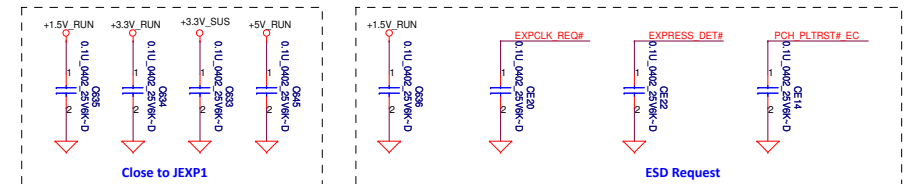
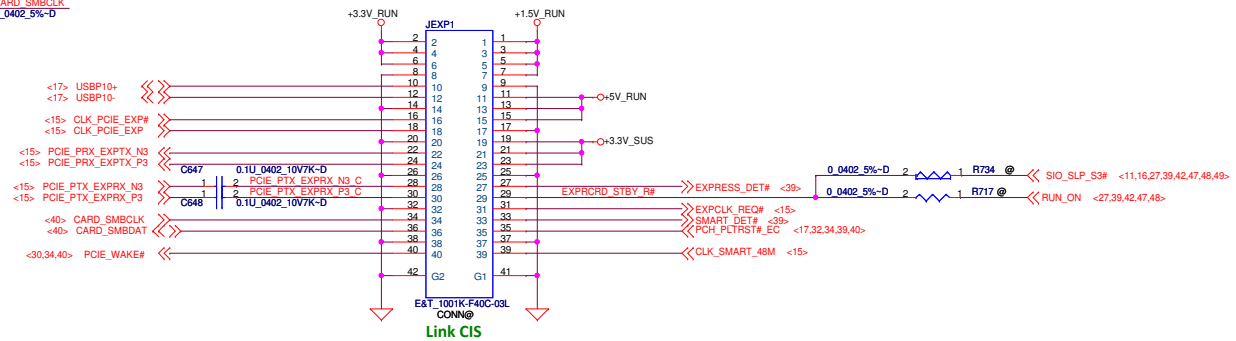
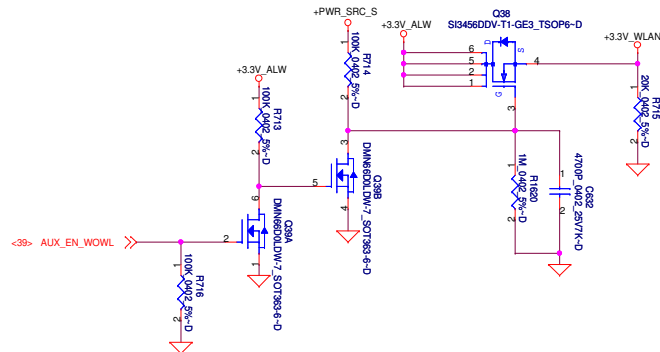
Sheet 33 of 61

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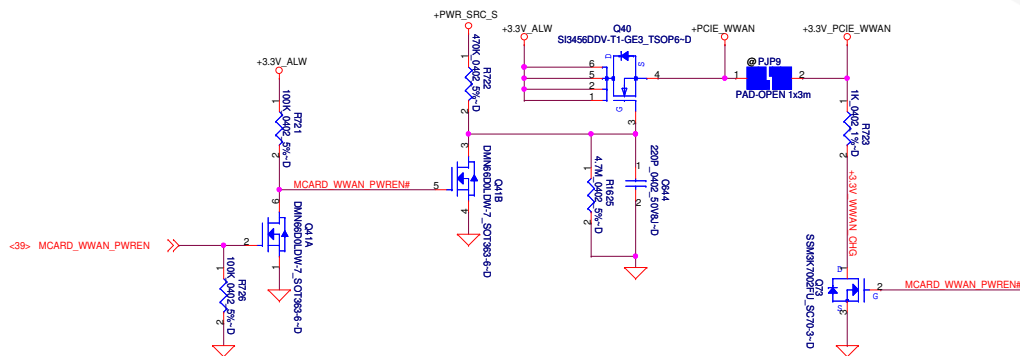
Express/Smart Card Conn.



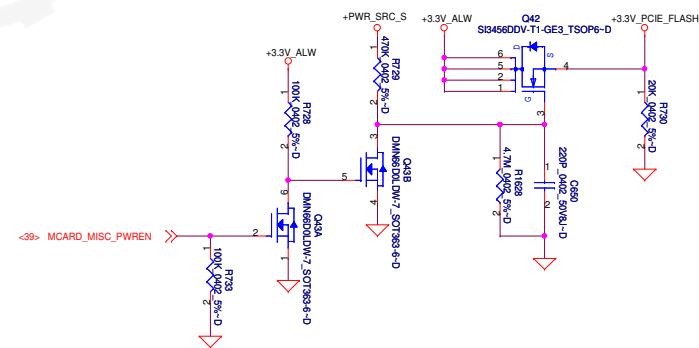
Power Control for Mini card2



Power Control for Mini card1



Power Control for Mini card3



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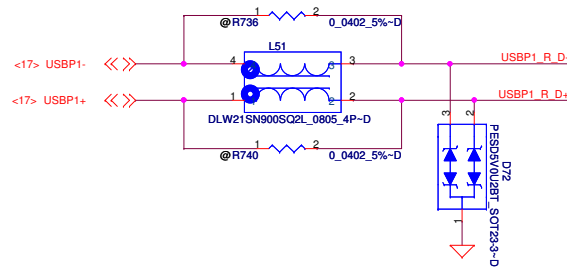
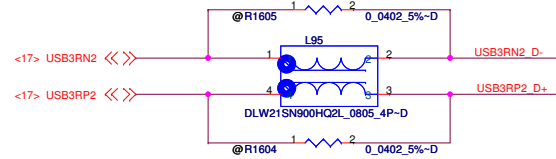
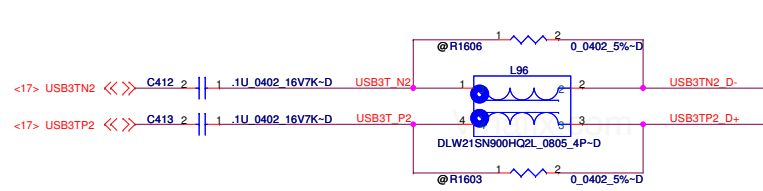
MINI CARD PWR/EXP SC

Number
LA-7901P

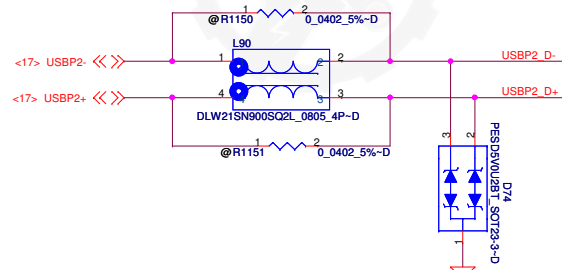
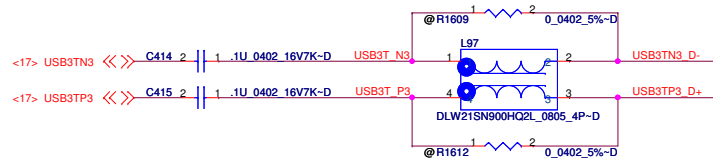
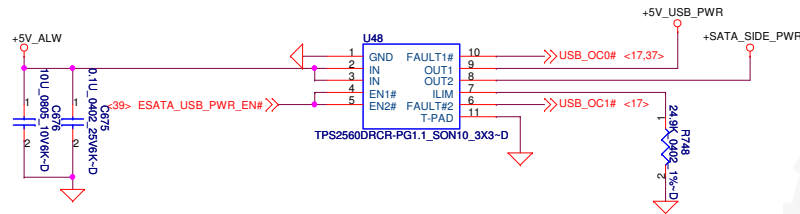
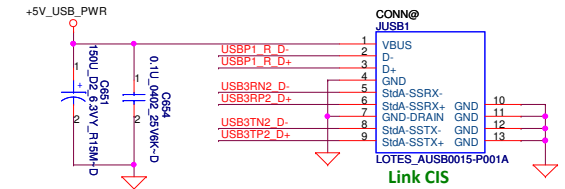
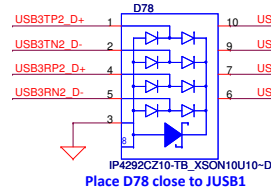
Date: Friday, March 02, 2012

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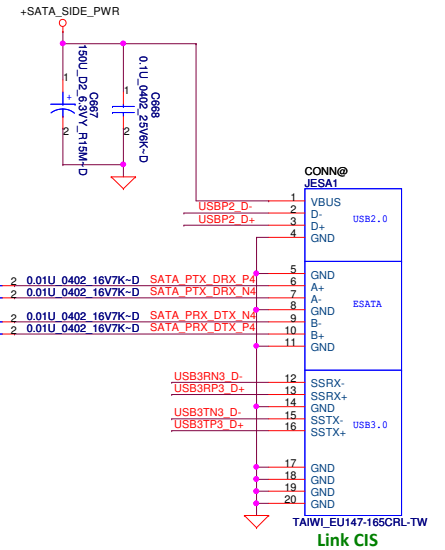
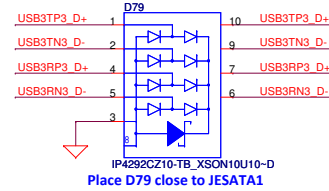
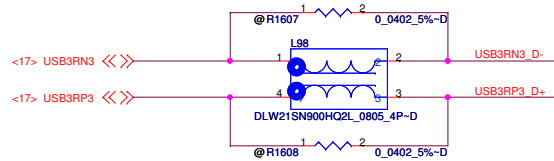
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Place D72 close to JUSB1



Place D74 close to JESATA1

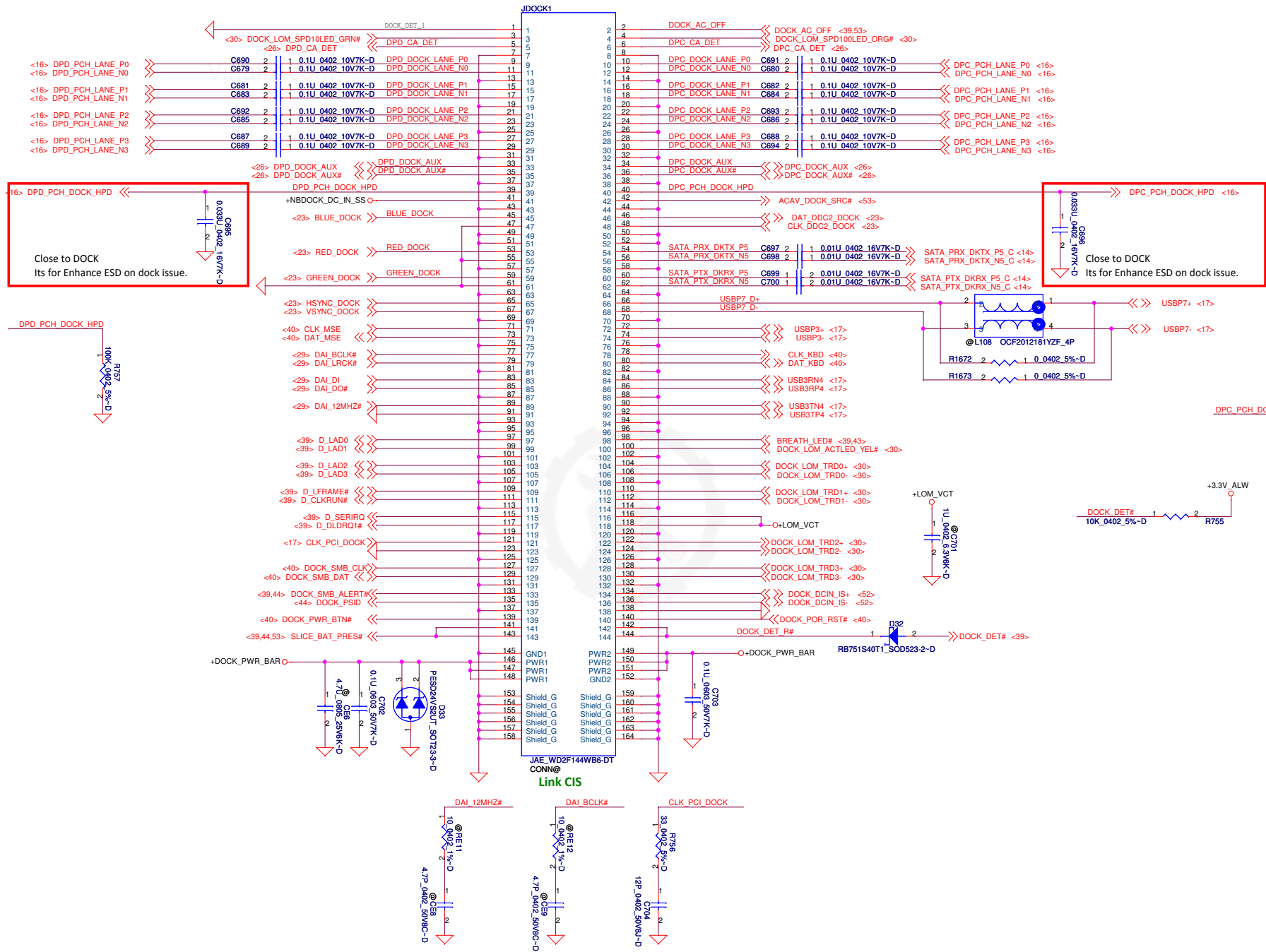


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| Title | | | |
| USB2.0/3.0 ESATA | | | |
| Size | | | |
| Document Number | | | |
| LA-7901P | | | |
| Date | | | |
| Friday, March 02, 2012 | | | |
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| Rev | | | |
| 1.0 | | | |

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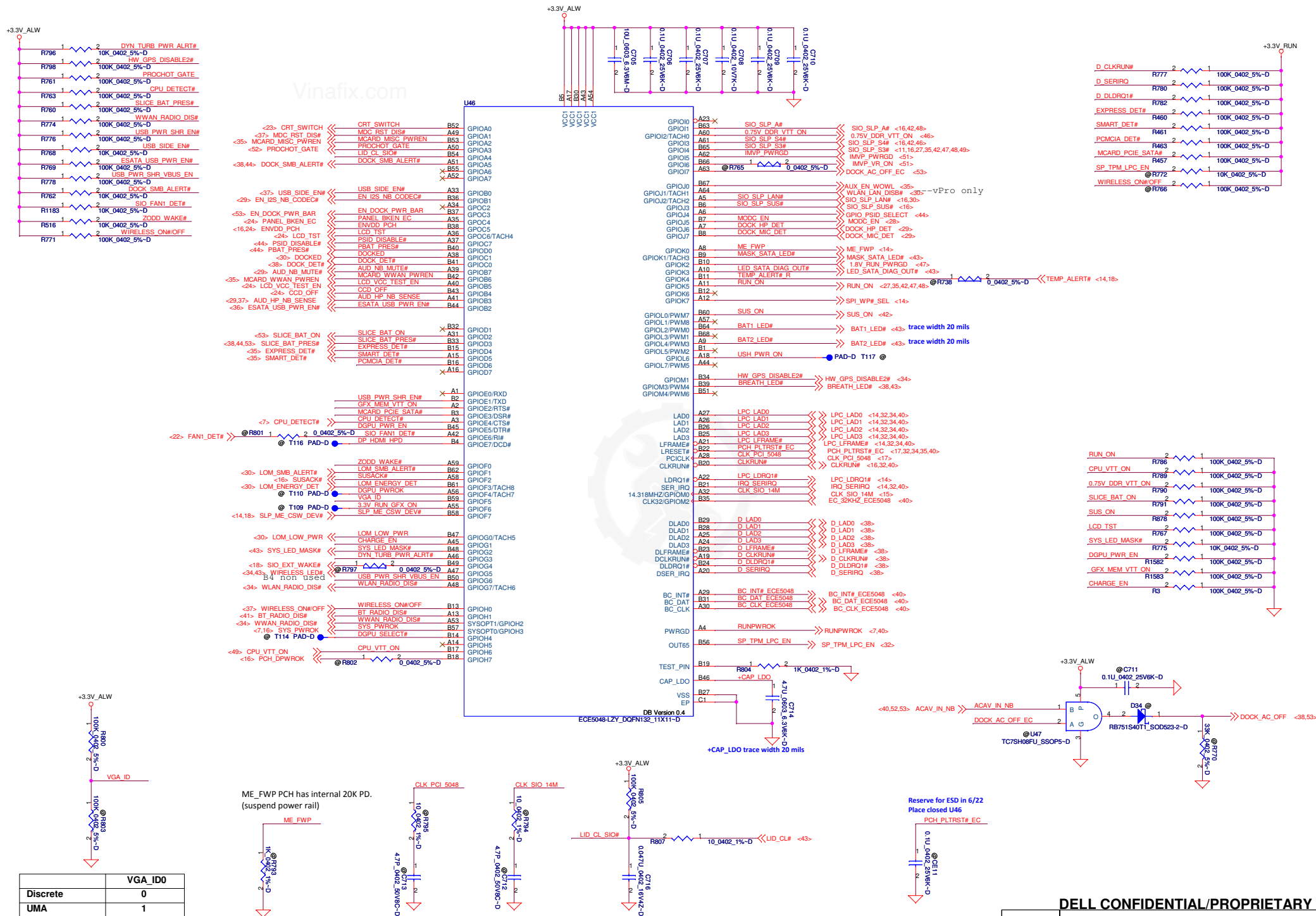


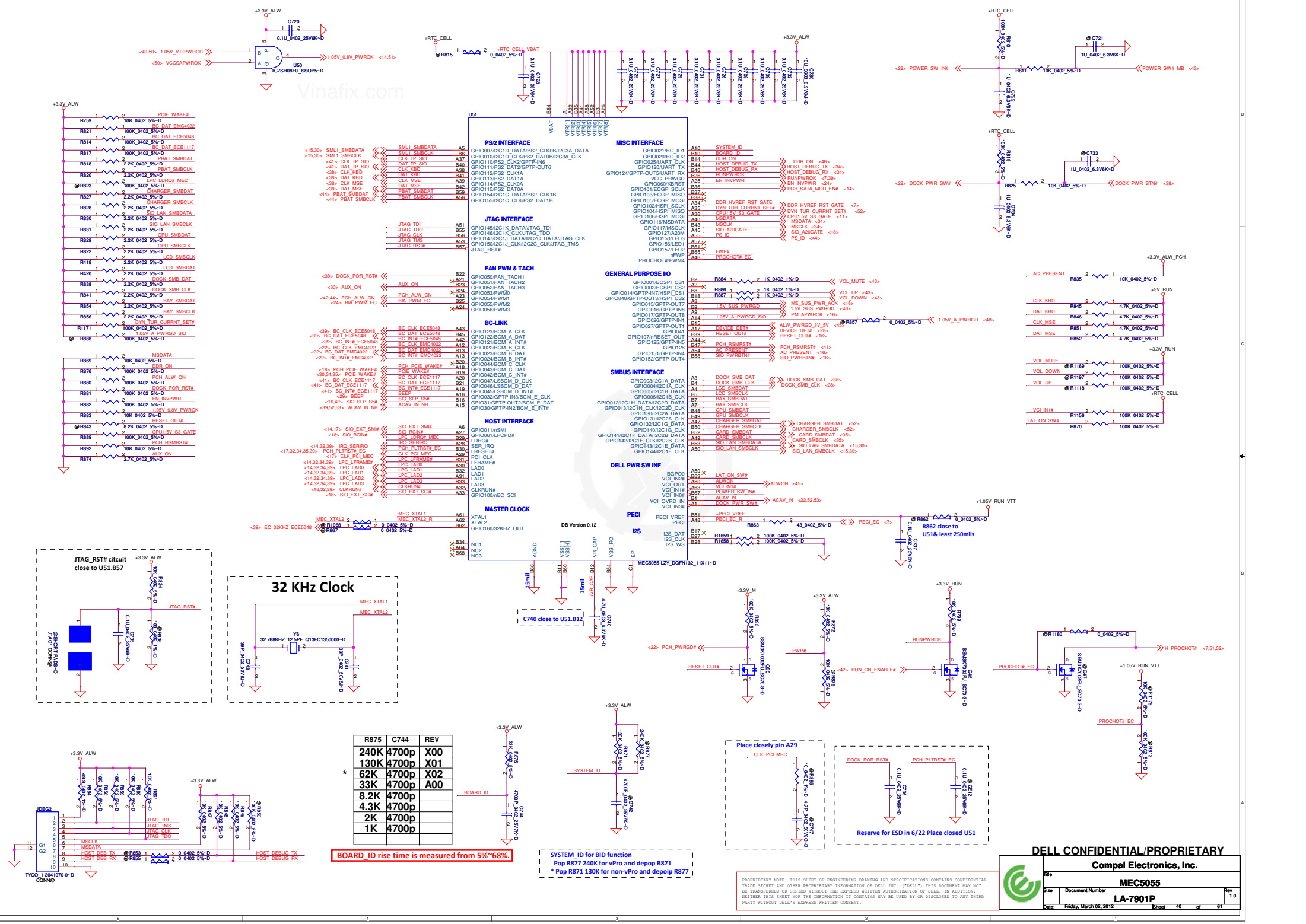
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|------------------------------|----------|-------|--|
| DOCKING CONN | | | |
| LA-7901P | Rev 1.0 | | |
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Vinafix.com

| R875 | C744 | REV |
|------|-------|-----|
| 240K | 4700p | X00 |
| 130K | 4700p | X01 |
| 62K | 4700p | X02 |
| 33K | 4700p | A00 |
| 8.2K | 4700p | |
| 4.3K | 4700p | |
| 2K | 4700p | |
| 1K | 4700p | |

BOARD_ID rise time is measured from 5%-68%.

SYSTEM_ID for BID function
Pop R877 240K for vPro and depop R871
Pop R871 130K for non-vPro and depop R877

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MEC5055

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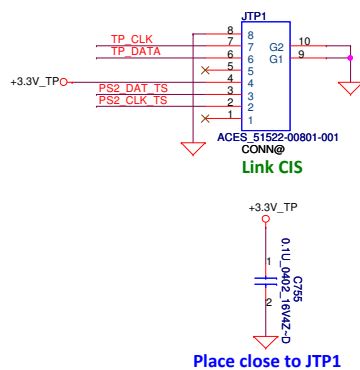
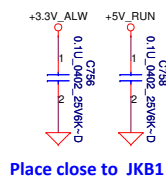
[illegible]

Diagram showing the connection of pins 1 through 12 of the Link C1S module. The connections are as follows:

- Pin 1: KB1
- Pin 2: PS2_CLK TS (KB_DET# <18>)
- Pin 3: PS2_DAT TS
- Pin 4: +3.3V_ALW
- Pin 5: +5V_RUN
- Pin 6: BC_INT#_ECE1117 <40>
- Pin 7: BC_DAT_ECE1117 <40>
- Pin 8: BC_CLK_ECE1117 <40>
- Pin 9: GND
- Pin 10: GND
- Pin 11: ACES_51524-0100N-001
- Pin 12: CONN@



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| | |
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|-----|-----|

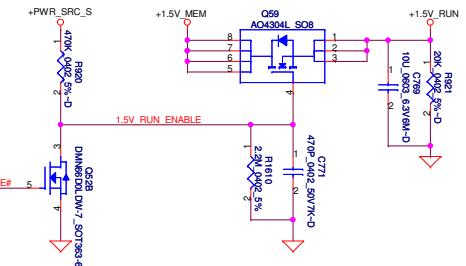
DC/DC Interface

<11,16,27,35,39,47,48,49> SIO_SLP_S3#
<27,35,39,47,48> RUN_ON

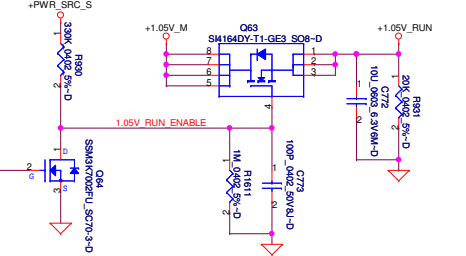
For SSI
w/ vpro: PJP7 open and PJP8 open
w/o vpro: PJP7 open and PJP8 short.depop Q63
For PT
w/o vpro: PJP7 and PJP8 open.pop Q63

Discharge Circuit

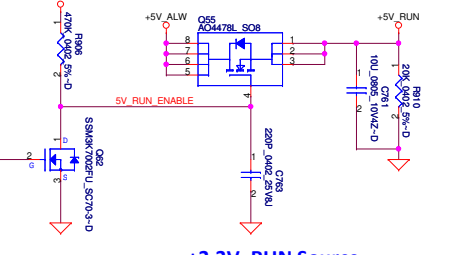
+1.5V_RUN Source



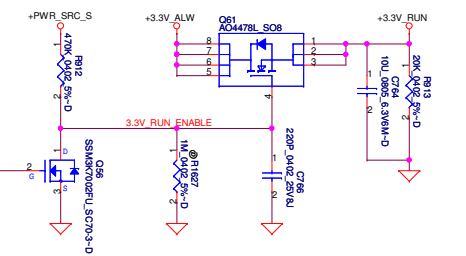
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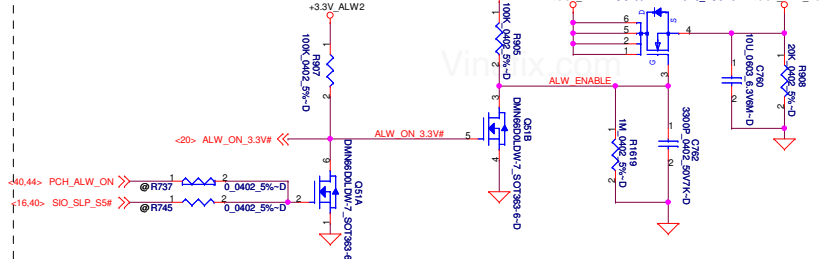
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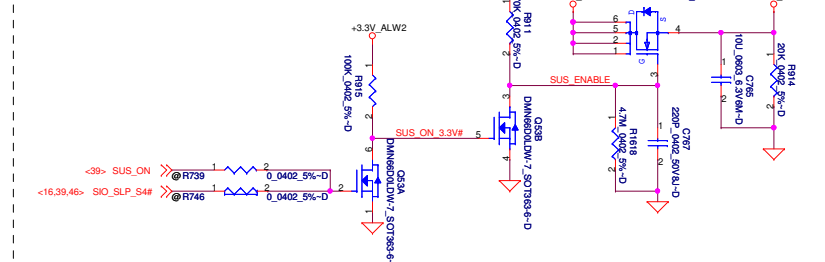
+3.3V_RUN Source



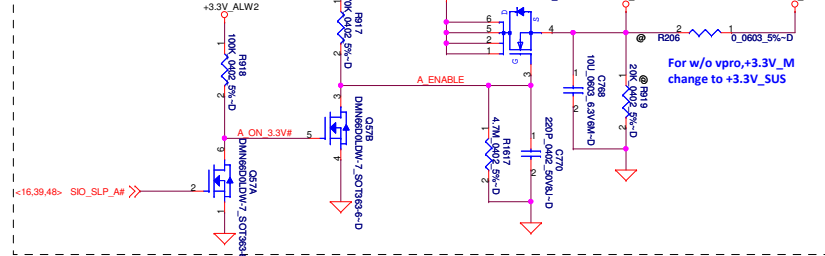
+3.3V_ALW_PCH Source



+3.3V_SUS Source



+3.3V_M Source



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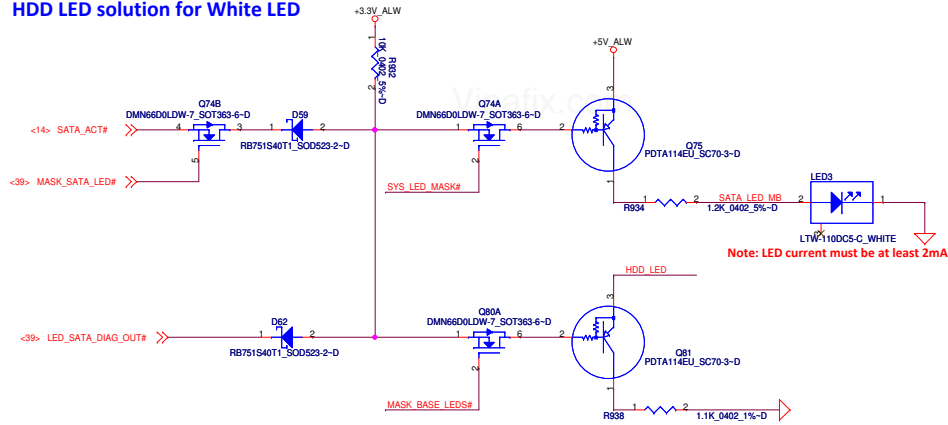
Compal Electronics, Inc.

POWER CONTROL

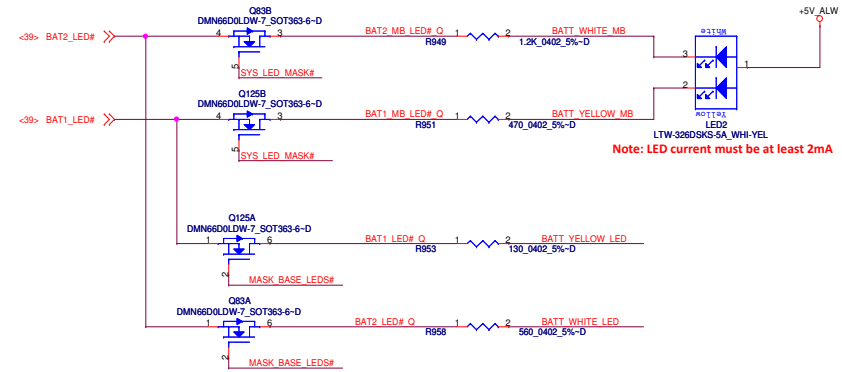
LA-7901P

| Rev | Rev | Rev |
|-------|------------------------|-------|
| 1.0 | 1.0 | 1.0 |
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| Date: | Friday, March 02, 2012 | |

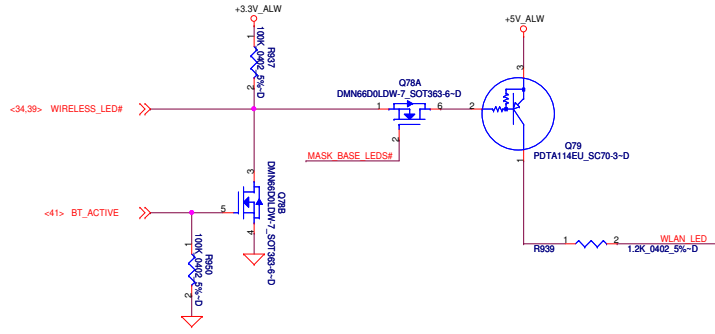
BDD LED solution for White LED



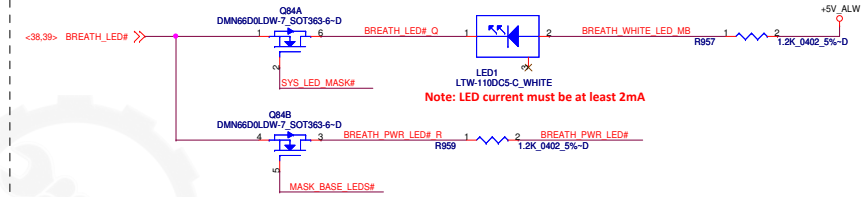
Battery LED



WLAN LED solution for White LED



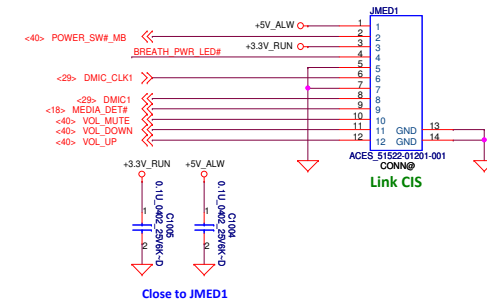
Breath LED



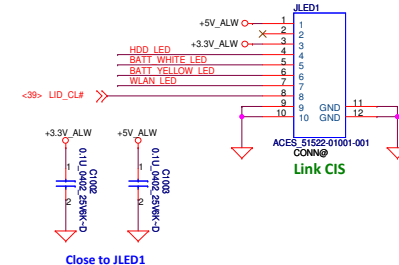
LED Circuit Control Table

| | SYS_LED_MASK# | LID_CL# |
|----------------------------------|---------------|---------|
| Mask All LEDs (Sniffer Function) | 0 | X |
| Mask Base MB LEDs (Lid Closed) | 1 | 0 |
| Do not Mask LEDs (Lid Opened) | 1 | 1 |

MEDIA BOARD

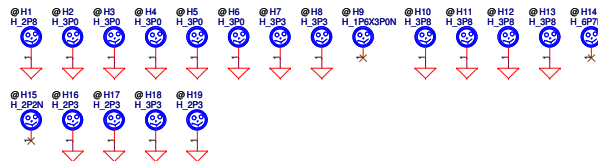


LED BOARD



Fiducial Mark

- FD1
- FIDUCIAL MARK-D
- FD2
- FIDUCIAL MARK-D
- FD3
- FIDUCIAL MARK-D
- FD4
- FIDUCIAL MARK-D



EMI CLIP



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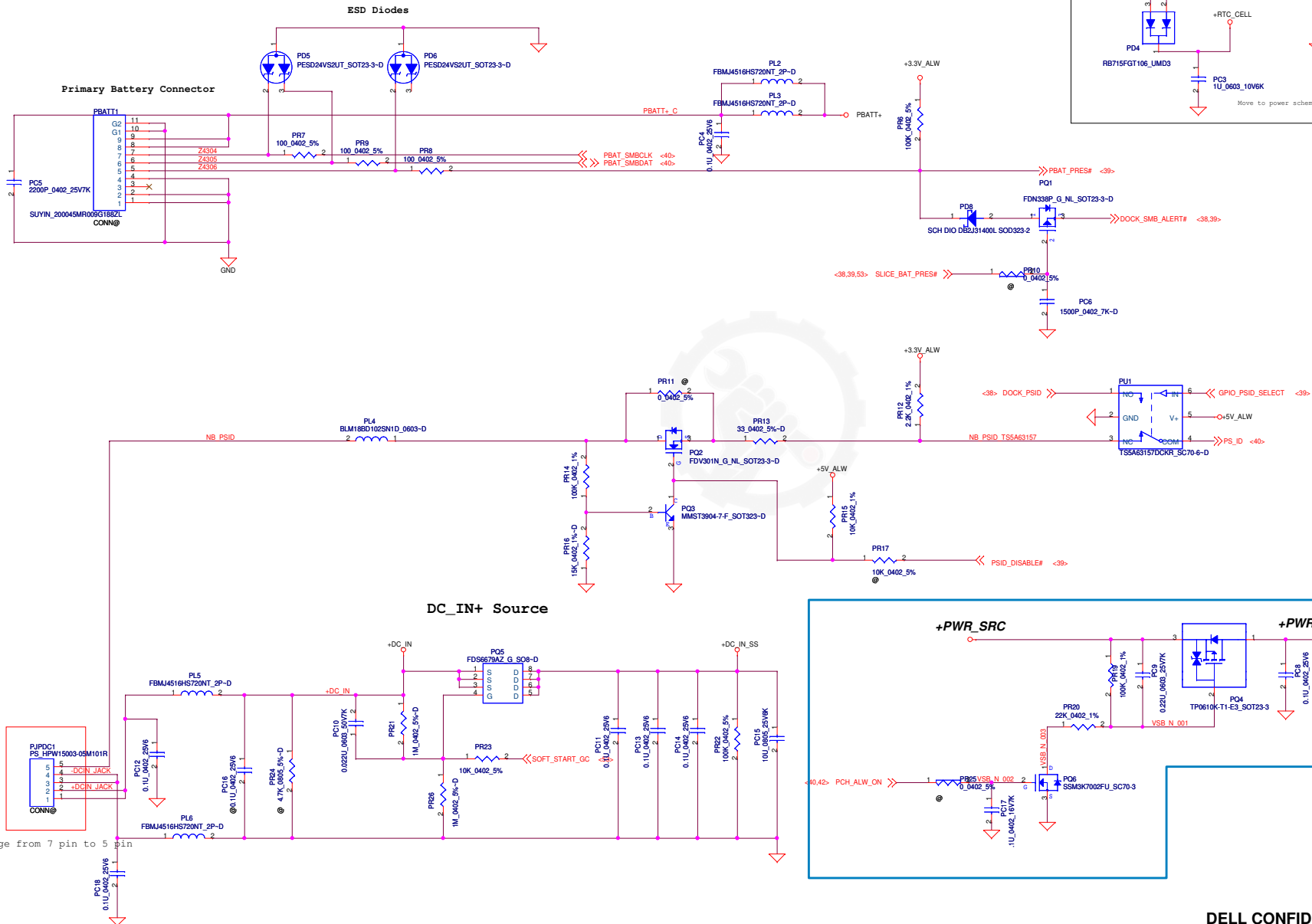
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PWR/LED Conn/PAD/ME

| | | |
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| Size | Document Number | Rev |
| LA-7901P | 1.0 | |

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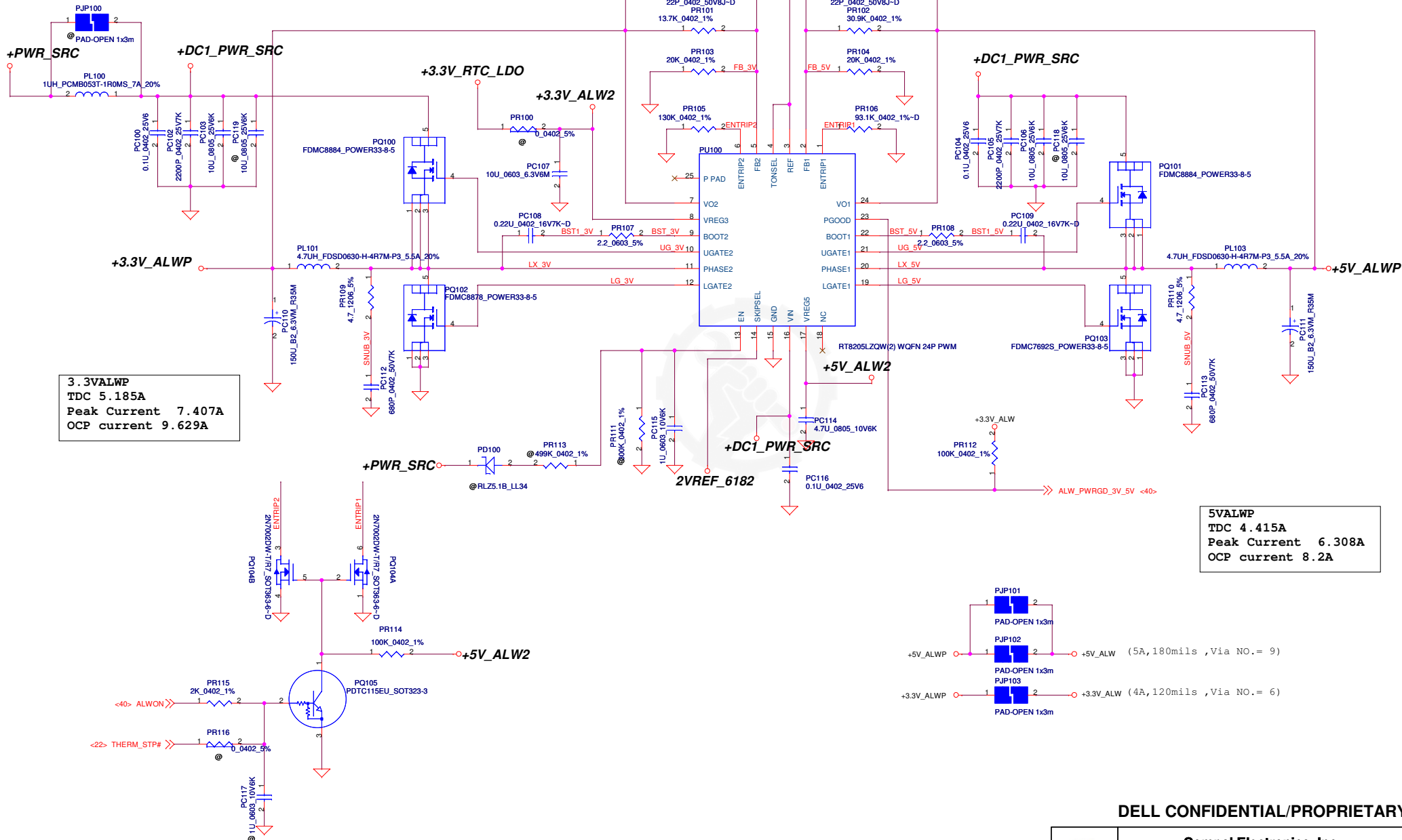
Compal Electronics, Inc.

+DCIN

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| | LA-7902P | 1.0 |
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2VREF_6182



3.3VALWP
TDC 5.185A
Peak Current 7.407A
OCP current 9.629A

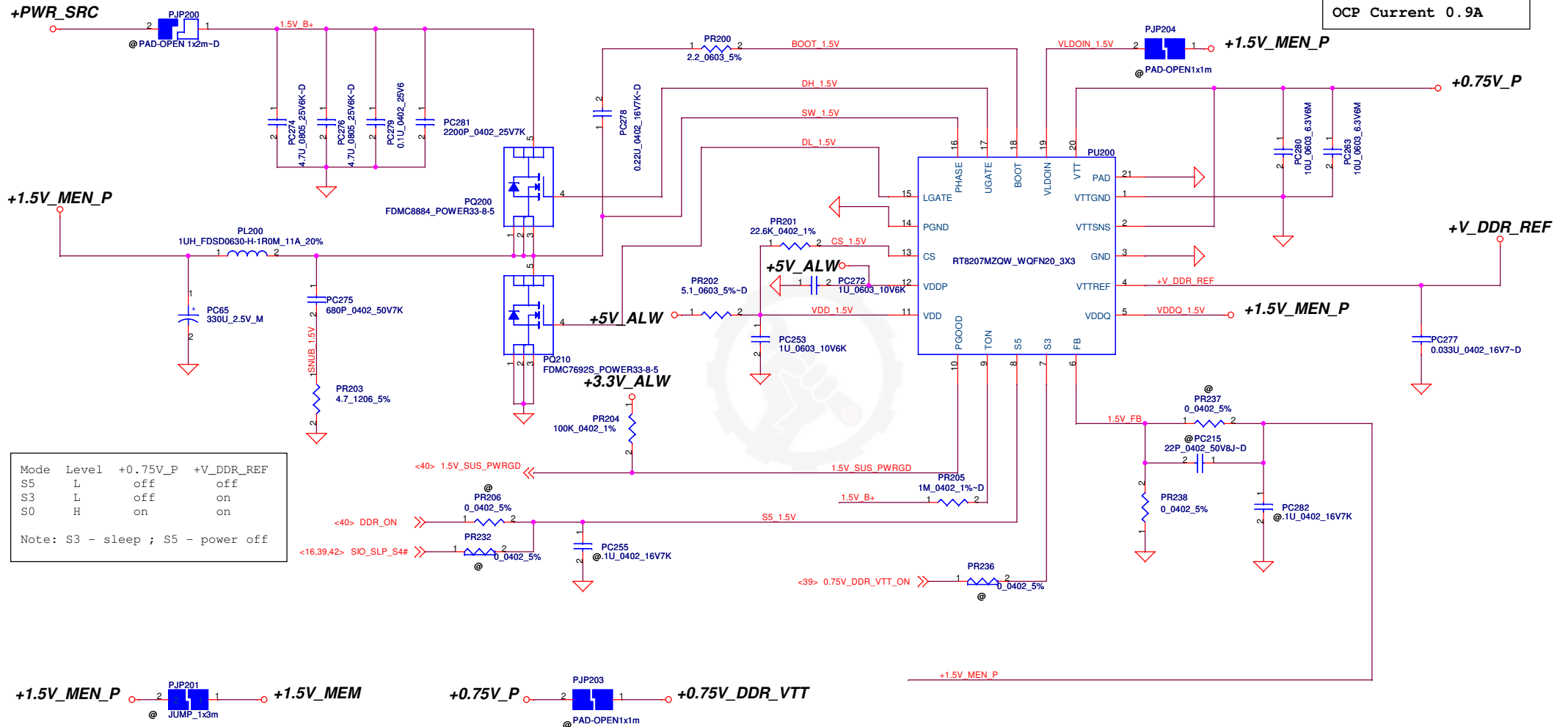
5VALWP
TDC 4.415A
Peak Current 6.308A
OCP current 8.2A

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| Compal Electronics, Inc. | | | |
|------------------------------|-----------------|-------|----------|
| Title | | | |
| +5V_ALW/3.3V_ALW | | | |
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| Date: Friday, March 02, 2012 | | Sheet | 45 of 61 |

0.75Volt +/- 5%
TDC 0.525A
Peak Current 0.75A
OCP Current 0.9A



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+1.5V MEN/+0.75V DDR VTT

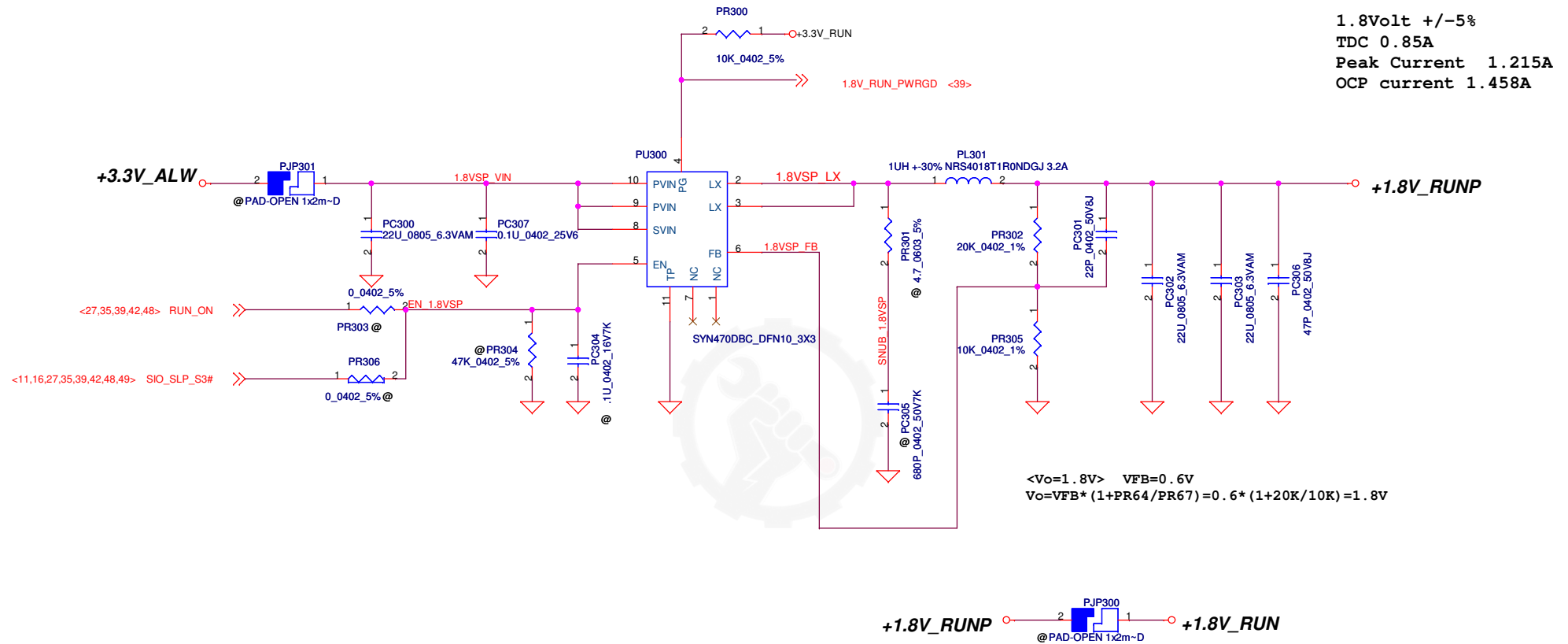
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| Rev | |
| 1.0 | |

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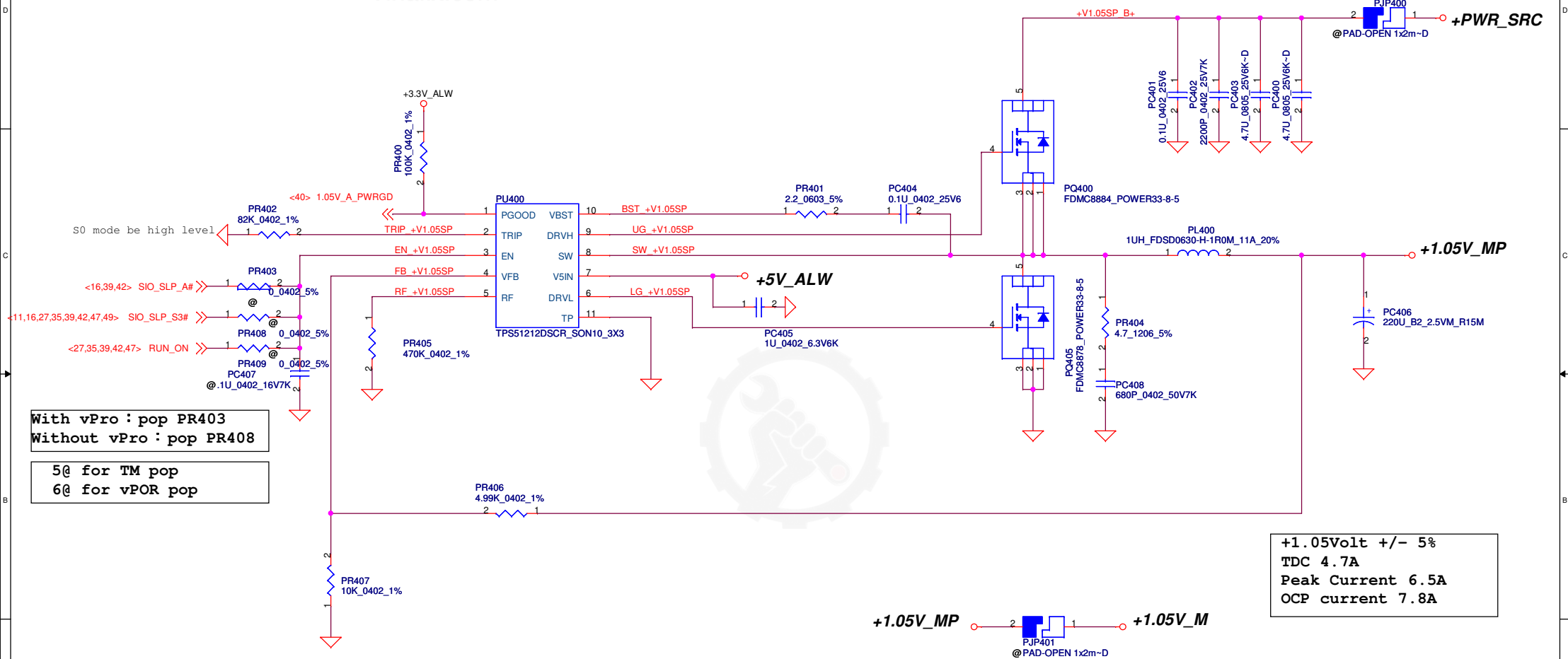
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| Compal Electronics, Inc. | | | |
|--------------------------|------------------------|------------------|----------|
| Title | | +1.8V_RUN | |
| Size | Document Number | LA-7902P | |
| Date: | Friday, March 02, 2012 | Sheet | 47 of 61 |
| | | Rev | 1.0 |

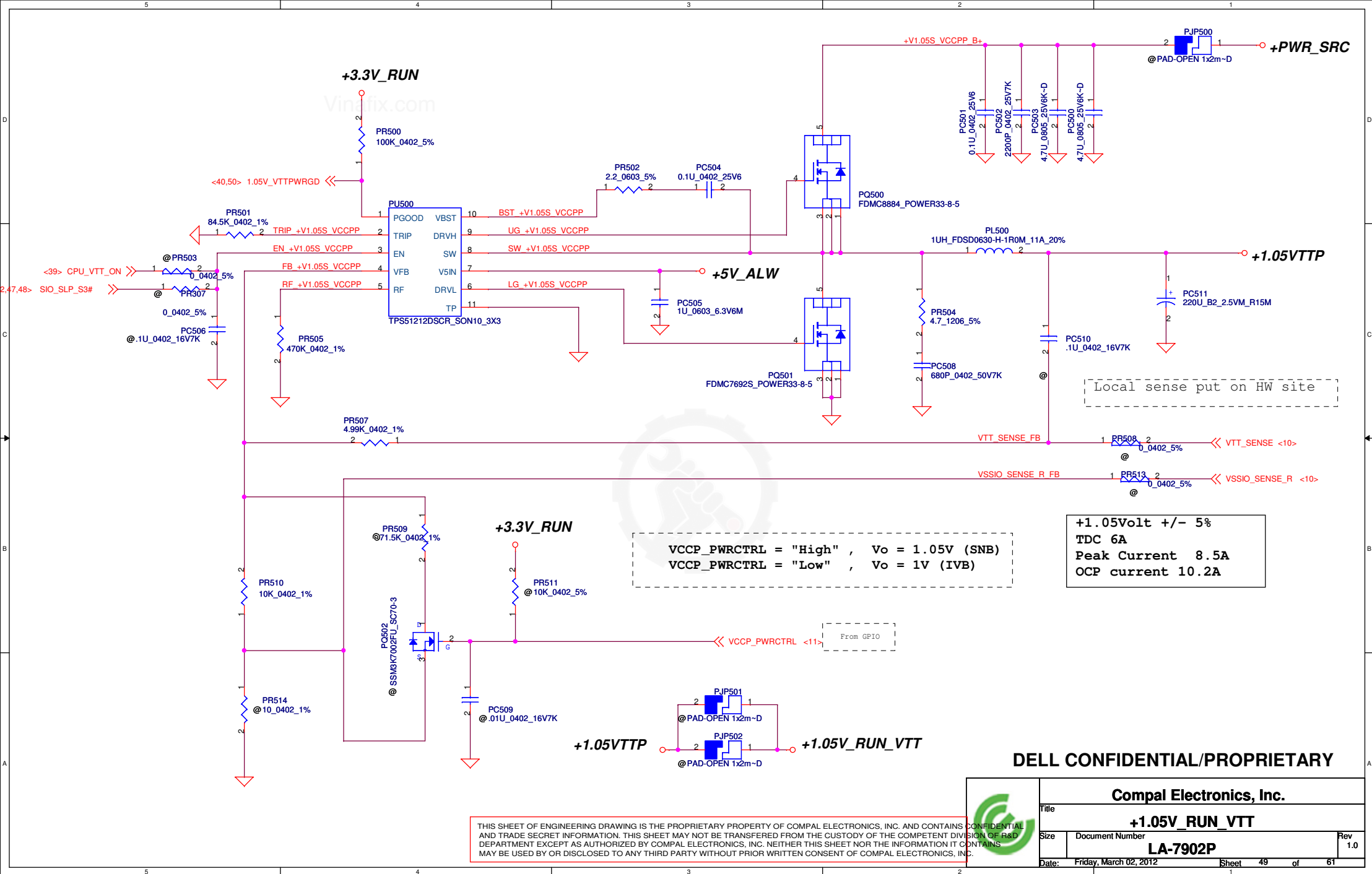


+1.05Volt +/- 5%
TDC 4.7A
Peak Current 6.5A
OCP current 7.8A

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|--------------------------|------------------------|--|----------------|
| Title | | | |
| +1.05V_M | | | |
| Size | Document Number | | Rev |
| | LA-7902P | | 1.0 |
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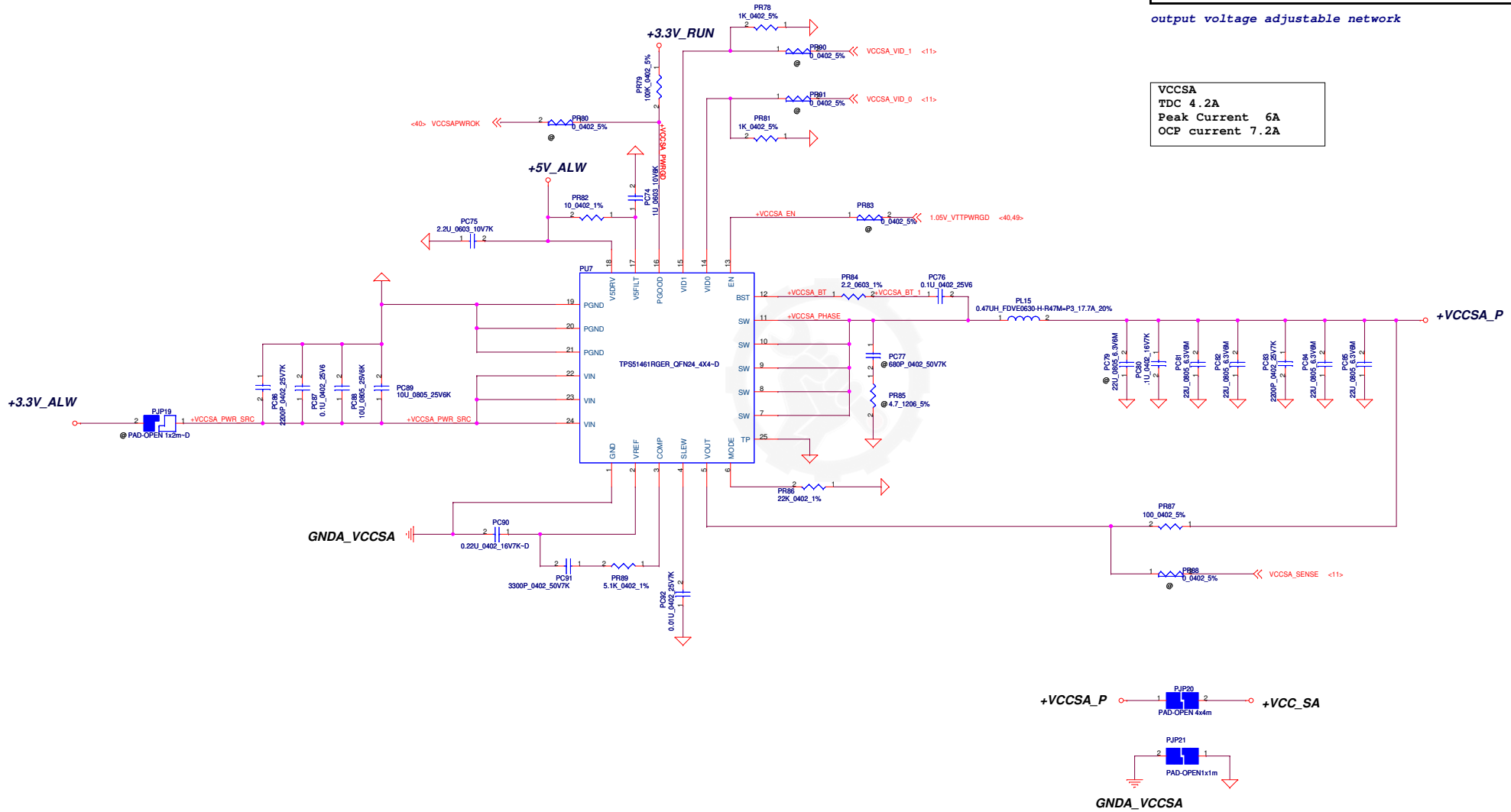


The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

| VID [0] | VID[1] | VCCSA Vout |
|---------|--------|------------|
| 0 | 0 | 0.9V |
| 0 | 1 | 0.8V |
| 1 | 0 | 0.725V |
| 1 | 1 | 0.675V |

output voltage adjustable network

| |
|------------------|
| VCCSA |
| TDC 4.2A |
| Peak Current 6A |
| OCP current 7.2A |



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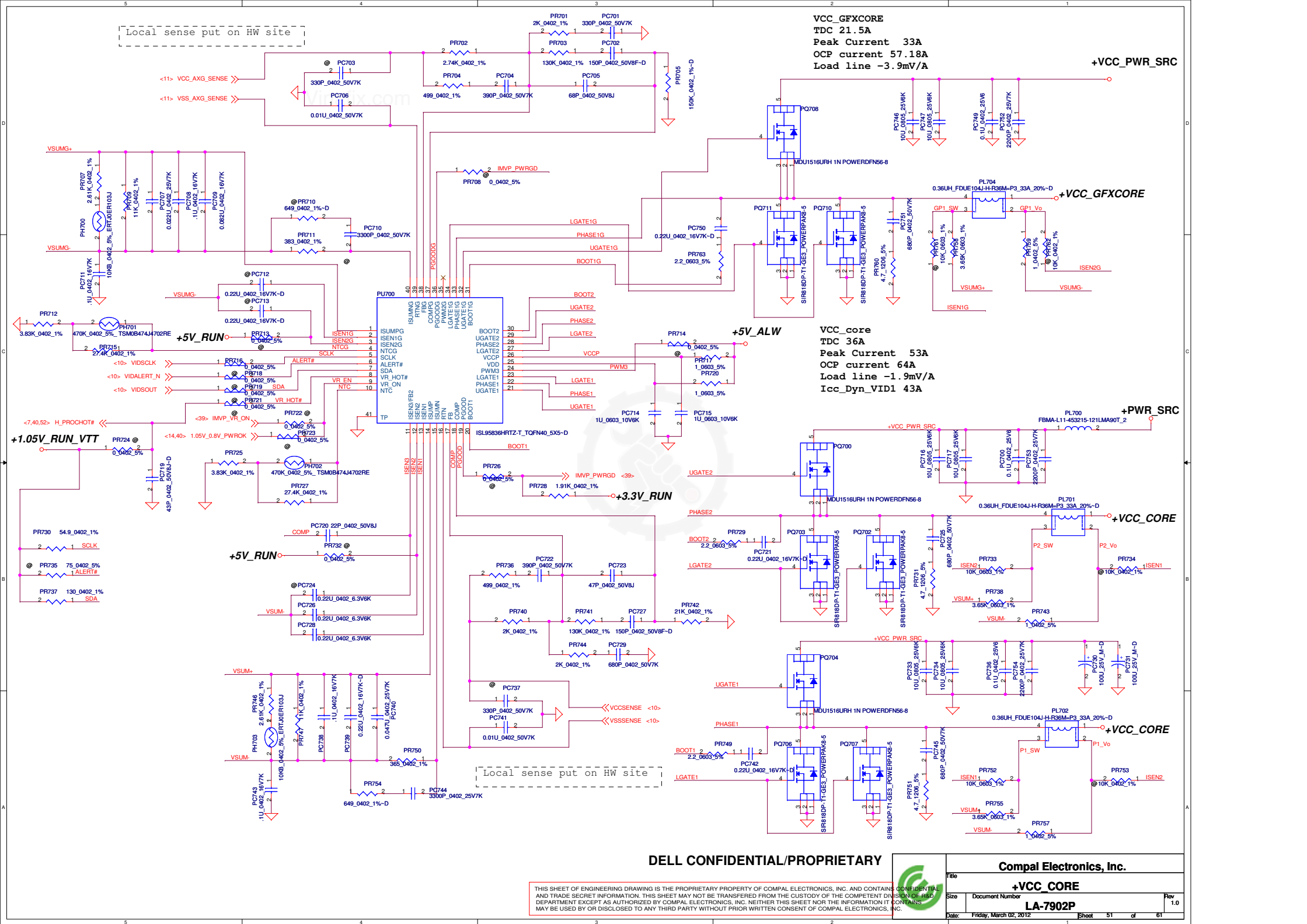
+VCC_SA

| | |
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| Size | Document Number |
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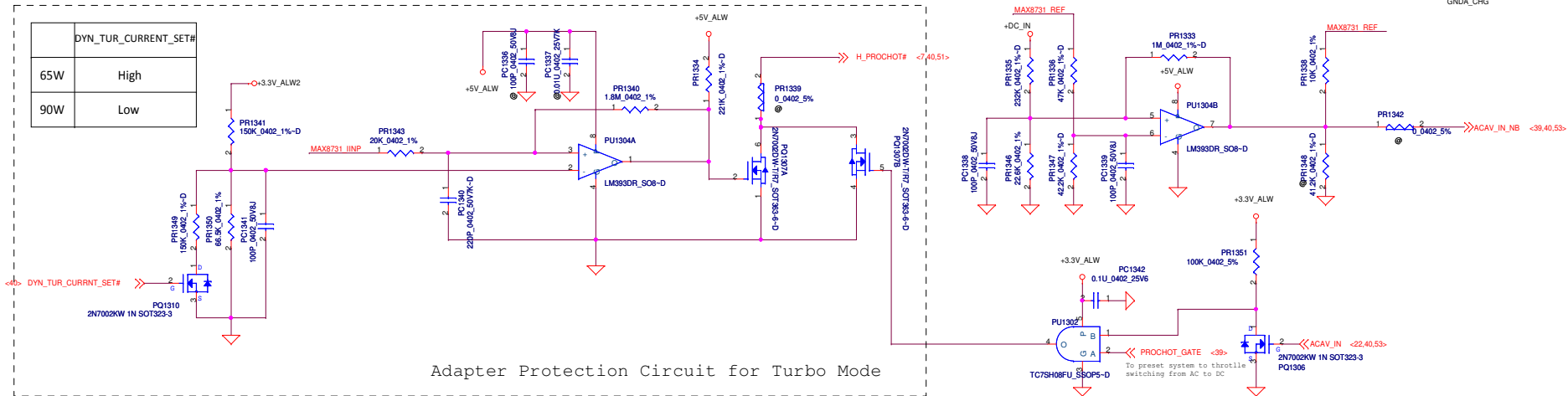
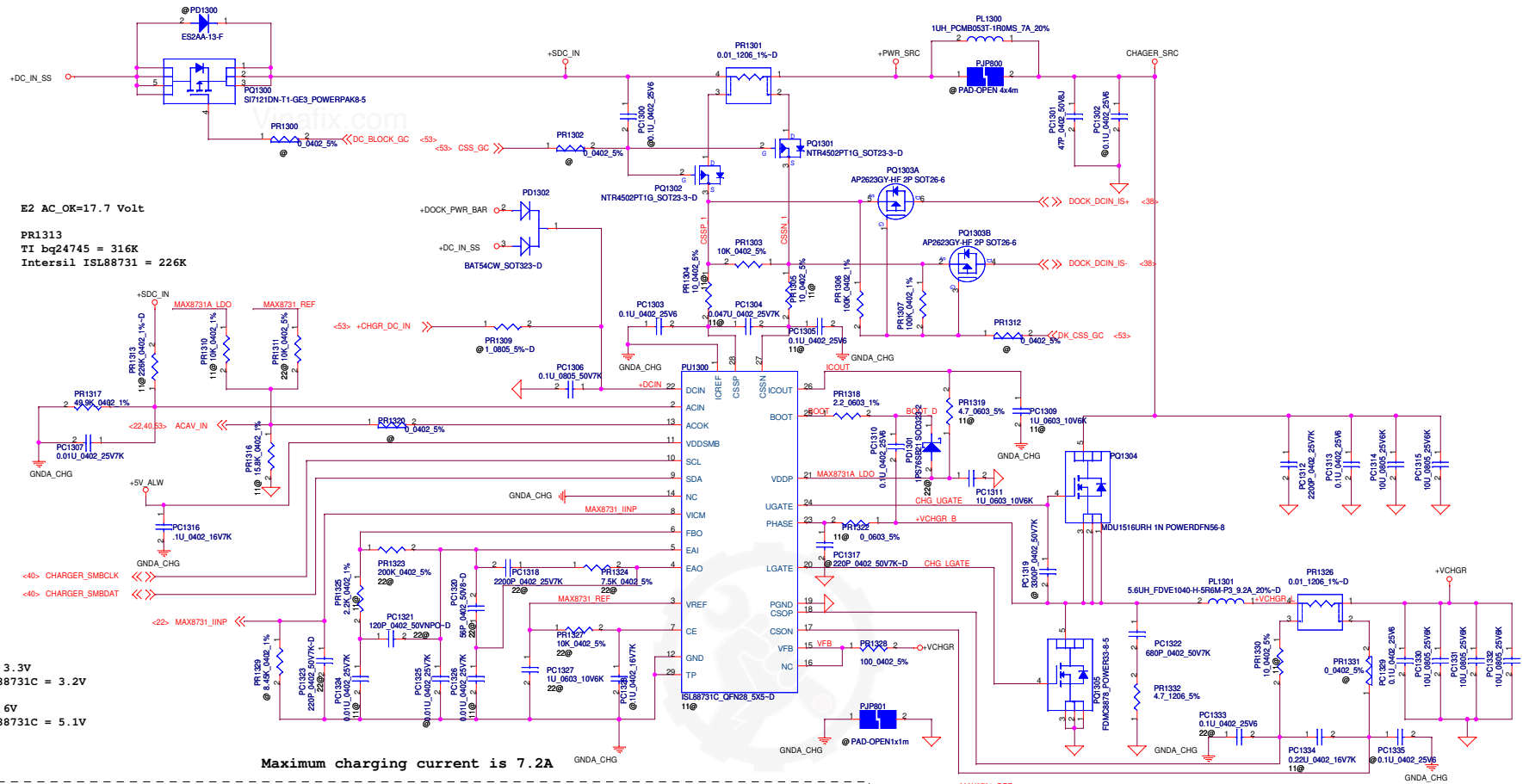
Date: Friday, March 02, 2012

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1.0



ISL88731C 11@
BQ24747 22@

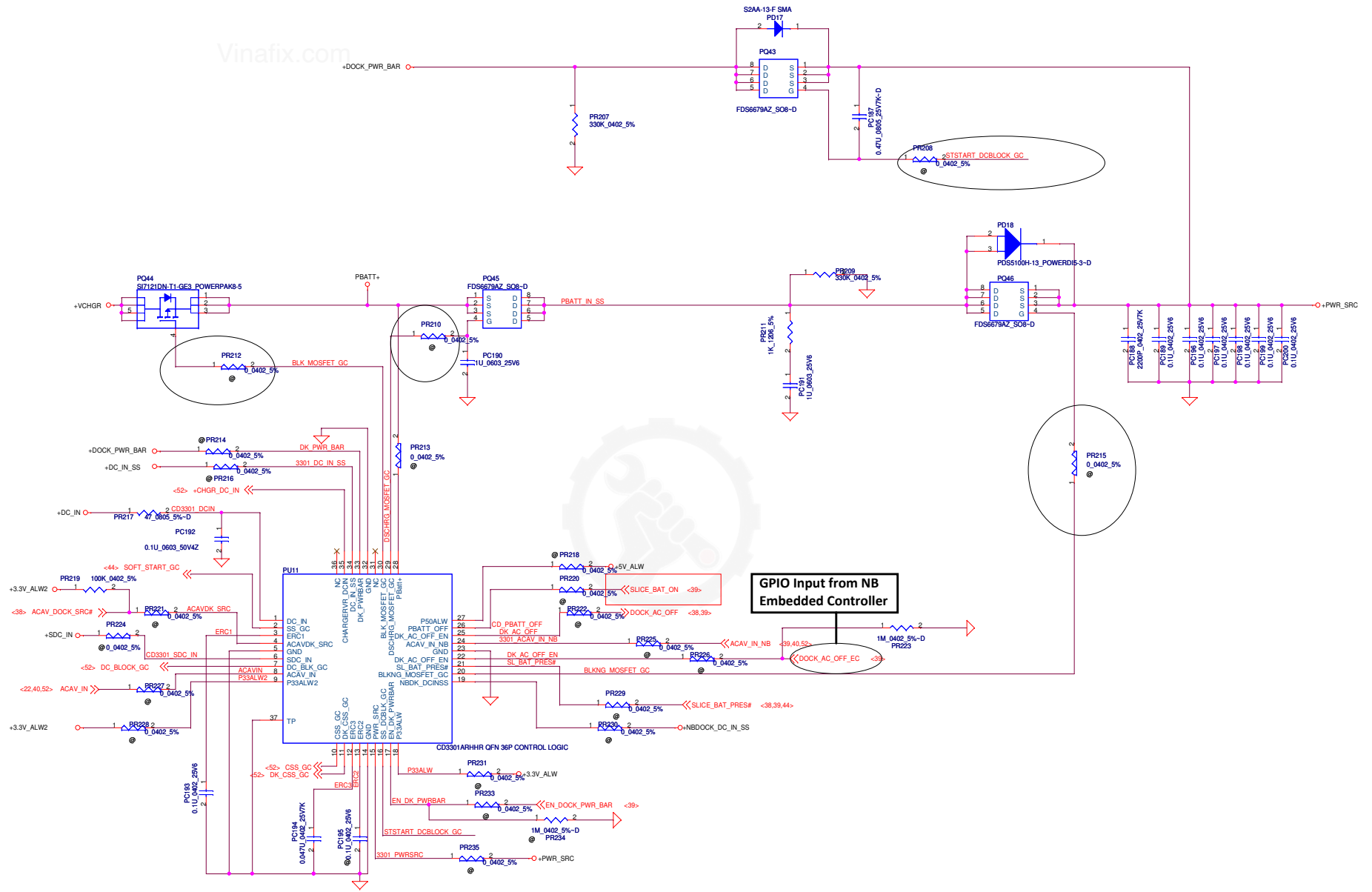


| | | | | | | | | |
|------------|--------------|--------------|----------------|------------|------------|------------|---------------------------|------------|
| PDI300 22@ | PR1313 22@ | PR1325 22@ | PC1334 22@ | PR1330 22@ | PR1304 22@ | PR1305 22@ | PC1304 22@ | PR1322 22@ |
| BQ24747 | 316k_0402_1% | 4.7k_0402_1% | 0.1u_0402_25V6 | 0_0402_5% | 0_0402_5% | 0_0402_5% | 0.1u_0402_25V6 1+-5% 0603 | |

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|--------------------------|------------------------|
| Compal Electronics, Inc. | |
| Charger | |
| File | Document Number |
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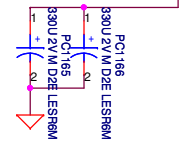
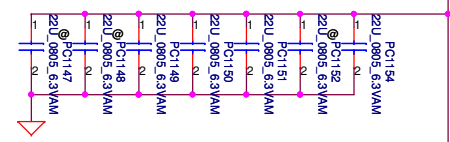
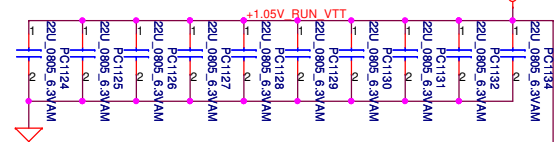
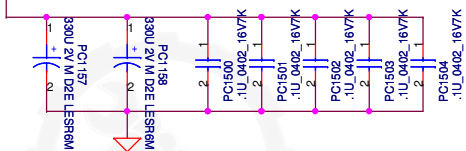
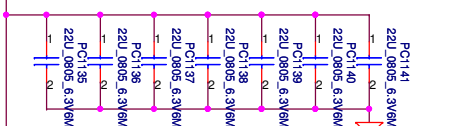
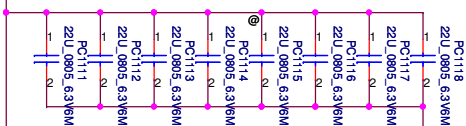
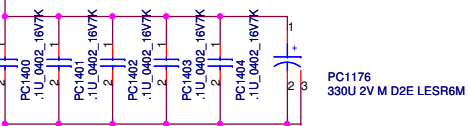
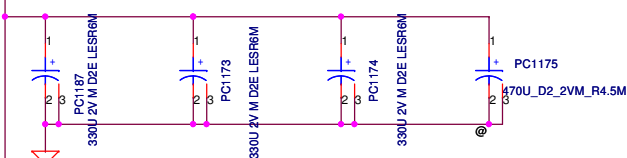
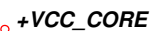
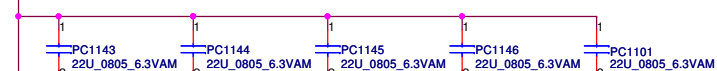
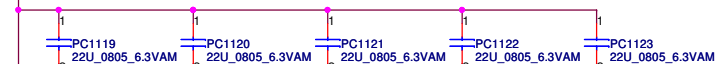
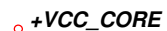
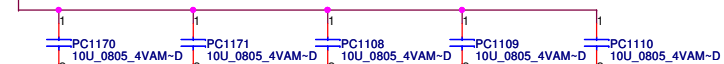
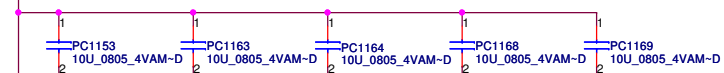
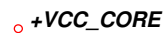
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Selector

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Compal Electronics, Inc.

Title

PROCESSOR DECOUPLING

Size

Document Number

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1.0

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Version Change List (P. I. R. List)

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| Item | Page# | Title | Date | Request Owner | Issue Description | Solution Description | Rev. |
|------|----------|-------|------|---------------|--|--|------|
| 1 | 44 | Power | 8/18 | Compal | ME design change. | PJPDC1 change from 7pin to 5pin | X01 |
| 2 | 45 | Power | 8/18 | Compal | Main and 2nd IC common setting. | De-pop PD100,PR113,PR111 | X01 |
| 3 | 45 46 | Power | 8/18 | Compal | Prevent Jitter issue. | Add PC120,PC121,PC215 parallel with PR101,PR102,PR207 | X01 |
| 4 | 51 | Power | 8/18 | Compal | Prevent output voltage glitch when power up. | PU700 VCCP and VDD change form +5V_RUN to +5V_ALW | X01 |
| 5 | 53 | Power | 8/18 | Dell | Change net name PBATT to SLICE_BAT_ON. | Change net name same as E4. | X01 |
| 6 | 50 | Power | 8/18 | Compal | Reserve 0 ohm resistance for test. | Add PR90, PR91 | X01 |
| 7 | 45 52 | Power | 8/30 | Compal | For reduce EMI radiation. | Pop PL100, PL1300 | X01 |
| 8 | 54 | Power | 8/30 | Compal | Reserve cap for improve transient response. | Reserve PC1176 | X01 |
| 9 | 53 | Power | 8/30 | Compal | For reduce EMI radiation. | Add PC196, PC197, PC198, PC199, PC200 | X01 |
| 10 | 54 | Power | 8/31 | Compal | Change to green P/N. | Change PQ4, PC1153, PC1163, PC1164, PC1168, PC1169, PC1170, PC1171, PC1108, PC1109, PC1110, PC1187, PC1173, PC1174, PC1175, PC1157, PC1158, PC179, PQ1310, PQ1306 to green P/N | X01 |
| 11 | 48 | Power | 9/1 | Dell | For support TL+TM | Change 6@ to pop for PC400~PC406, PC408, PL400, PQ400, PQ405, PR400~PR407, PU400. 5@ to @ for PR408. | X01 |
| 12 | 49 | Power | 9/1 | Compal | For fix 1.05V_RUN_VTT on 1.05V | Depop PR509, PR511, PQ502. Change PR507 to 4.99k. | X01 |
| 13 | 51 | Power | 9/5 | Compal | Follow EMI requirement. | Change PL700 to SM01000DJ00 | X01 |
| 14 | 45 46 | Power | 9/6 | Compal | Change to green P/N. | Change PC107, PC263, PC280, PC405, PC505 to HF P/N. | X01 |
| 15 | 52 | Power | 9/13 | Compal | For reduce EMI radiation. | Pop PC1400~1404, PC1500~PC1504. | X01 |

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| 16 | 51 | Power | 9/14 | Compal | Adjust CPU transient , loadline and OCP | Add PC740 to 0.1uF Change PR750 to 365 ohm Change PR741 to 130K ohm Change PC744 to 3300pF, PR754 to 649ohm. | X01 |
| 17 | 51 | Power | 9/14 | Compal | Adjust AXG transient , loadline and OCP | Change PR703 to 130K ohm Change PC709 to 82nF Change PR702 to 2.74K ohm Change PR711 to 383 ohm | X01 |
| 18 | 52 | Power | 11/17 | Compal | Shortage issue | Change PQ1303 from NTGD416 to AP2623 | X02 |
| 19 | 52 | Power | 11/17 | Compal | Need ESD protected | Change PQ1306, PQ1310 from SB57002040L to SB000009Q80 | X02 |
| 20 | 53 | Power | 11/17 | Compal | IC version upgrade | Change PU11 from CD3301 to CD3301A | X02 |
| 21 | 45 | Power | 11/17 | Compal | Shortage issue | Change PC110, PC111 from SGA00004E00 to SGA00002N80 | X02 |
| 22 | 45 | Power | 11/17 | Compal | EMI request | Pop PC1138, PC1139, PC1149, PC1150 | X02 |
| 23 | 44 | Power | 11/21 | Compal | Erp lot6 tier2 Fail issue | PWR_SRC_S control signal change from +3.3V_ALW to PCH_ALW_ON | X02 |
| 24 | 44 | Power | 12/05 | Compal | Prevent COS. | Change PD8 from SCS0340L01L to SCS00005C00 Change PD1301 from SCS00003M0L to SCS0000400L | X02 |
| 25 | 54 | Power | 12/13 | Compal | Prevent COS. | Change PC1176, PC1174, PC1173, PC1187, PC1157, PC1158, PC1165, PC1166 to SGA00002U1L | X02 |
| 26 | 50 | Power | 12/13 | Compal | Improve efficiency | change PR86 to 22K_0402_5% | X02 |
| 27 | 47 | Power | 12/16 | Compal | Prevent COS. | Change PL301 from SH00000MN00 to SH00000MW00 | X02 |

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|---------------|---------------|---------------|-----------------------|-------------------|---|--|----------------|
| 1 | 11 | HW | 08/25/2011 | COMPAL | INTEL review feedback | Add CC178,CC179,CC149,CC150 | X01 |
| 2 | 14, 39 | HW | 08/25/2011 | COMPAL | SMSC request to delete LPC_LDRQ0# | Leave LDRQ0# no connection on both of 5048 and PCH side Removed R743 | X01 |
| 3 | 22 | HW | 08/25/2011 | COMPAL | Removed reserve circuit for EMC4022 | Removed R405,C280,R392,R394 | X01 |
| 4 | 42 | HW | 08/25/2011 | COMPAL | Load SW sources output rising time mismatch and COS. cost concern | Change back to E3 +3.3V/5V_RUN discrete solution Removed U78 and add Q55,Q61 circuit | X01 |
| 5 | 29 | HW | 08/25/2011 | COMPAL | Codec is change to 92HD93 | Pop R162~R166 and de-pop U73,R1540 | X01 |
| 6 | 29 | HW | 08/25/2011 | COMPAL | Reserve so lay with ALC290 | Pop option for 92HD93/ALC290=>R1646/C1164; R1644/R1643; C965/R1642; Q107/R171 Reserve for ALC290 only: C1204, C1205, R1647, C1165, R1648 Reserve for 92HD93 only: R1645, C963 Add R174 depop and R175 pop | X01 |
| 7 | 20 | HW | 08/25/2011 | COMPAL | Vgs less than cut-in voltage in battery mode | Add control circuit QH6,R279,CH107 for +5V_ALW_PCH | X01 |
| 8 | 27, 28 | HW | 08/25/2011 | COMPAL | Vgs of 5V MOS maybe large than max rating | Add R517, R518 | X01 |
| 9 | 11 | HW | 08/25/2011 | COMPAL | Follow INTEL PDDG 0.8 | De-pop RC140 | X01 |
| 10 | 40 | HW | 08/25/2011 | COMPAL | Change board ID to X01 | Change R875 to 130Kohms | X01 |
| 11 | 34 | HW | 08/25/2011 | COMPAL | PCH GPIO52 need 8.2~10K pull up +3.3VS | Change R695 from 100K to 10Kohms | X01 |
| 12 | 23 | HW | 08/25/2011 | COMPAL | CRT SW 2nd source TI, TS3V713 pin29 is VDD | Connect U18 pin29 to +3.3V_RUN | X01 |
| 13 | 16 | HW | 08/25/2011 | COMPAL | +1.05V_M turn off before APWROK de-assert | Add UH5,CH108 6@ circuit reserve for VPRO | X01 |
| 14 | 41 | HW | 08/25/2011 | COMPAL | Reset IC threshold voltage issue | Change U4 to RT9801A (threshold adjustable) Add R1649~R1654;Reserve R1655 and pop R1623 | X01 |
| 15 | 26 | HW | 08/25/2011 | COMPAL | DPX_CA_DET voltage too low through dongle | Change U21 and U24 to SA000055G0L | X01 |
| 16 | 17, 18 | HW | 08/25/2011 | COMPAL | Request from INTEL review feedback | Pop RH332 for PCH_GPIO3 and RH180 for GPIO27 | X01 |
| 17 | 42 | HW | 08/25/2011 | COMPAL | Material changed | Power team request Q59 change to SB00000L80L | X01 |
| 18 | 43 | HW | 08/25/2011 | COMPAL | White light LED brightness is abnormal | Change R934, R938, R939, R949, R958, R957 and R959 to 1.2 Kohms | X01 |
| 19 | 40 | HW | 08/25/2011 | COMPAL | Reserve C1208 for ESD backup plan | Reserve C1208 for ESD backup plan | X01 |
| 20 | 11 | HW | 08/25/2011 | COMPAL | S3 can't resume issue | Control 1.5V_VDDQ by EC. Pop RC79 and de-pop RC82 | X01 |
| 21 | 17 | HW | 08/25/2011 | COMPAL | INTEL review feedback | Change RH331,RH272 to 10K ohm | X01 |

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| 22 | 34 | HW | 08/25/2011 | COMPAL | WWAN card request | JMINI1 pin 1 connect to PCIE_WAKE# | X01 |
| 23 | 14 | HW | 08/25/2011 | COMPAL | ROM size changed | Change U52 to 8M and R936,R895,R897,R900 to 6@ | X01 |
| 24 | 11 | HW | 08/25/2011 | COMPAL | Material package changed | Change CC161~CC166 from 0402 to 0603 | X01 |
| 25 | 42 | HW | 08/25/2011 | COMPAL | BOM changed | Change Q60 to 6@ | X01 |
| 26 | 39 | HW | 08/25/2011 | COMPAL | GPIO signal name changed same as E/P | Change PBATT_OFF to SLICE_BAT_ON | X01 |
| 27 | 34 | HW | 08/25/2011 | COMPAL | Material package changed | Changed C615 to SF000002000 | X01 |
| 28 | 30 | HW | 08/26/2011 | COMPAL | LAN EA result | Changed RL23 to 1.2K Ohm. | X01 |
| 29 | 40 | HW | 08/26/2011 | COMPAL | Backdrive issue | Depop R1169,R1197,R118 due to it has internal pull high. | X01 |
| 30 | 37 | HW | 08/29/2011 | COMPAL | To avoid power short to GND | NC Pin 15 for JAUD1 | X01 |
| 31 | 37 | HW | 08/30/2011 | COMPAL | Follow connector list | Swap JAUD1 pin. | X01 |
| 32 | 12 | HW | 08/30/2011 | COMPAL | Change part to HF part | Change QD1, QD2 part number to SB501380050 (for HF) | X01 |
| 33 | 15 | HW | 09/01/2011 | COMPAL | For clock EA | Change RH311 and RH314 to 10 ohm | X01 |
| 34 | 43 | HW | 09/01/2011 | COMPAL | ME drawing update | Add H19 | X01 |
| 35 | 14, 16 19, 22 30, 40 42 | HW | 09/01/2011 | COMPAL | BOM option change for TL | Change U53,R936,R895,R897,R900,RH350,UH5,CH108,RH116 RH202,R385,R426,R402,Q63,R931,Q58,Q60 R916,RL46,R871 to pop Change RH359,RH321,RH119,RH204,R430,R386,R408 ,R206,RL47,R877,to depop | X01 |
| 36 | 25 | HW | 09/02/2011 | COMPAL | Due to EMI HDMI test Fail, add EMI solution | Change resistor to Inductor Change R451, R459, R462, R466, R468, R469, R470, R471 to 9nH L99, L100, L101, L102, L103, L104, L105, L106. Add C1209, C1210, C1211, C1212, C1213, C1214, C1215 and C1216 between Inductor and HDMI connector | X01 |
| 37 | 37 | HW | 09/05/2011 | COMPAL | ME connector list change | Change JAU1 to 50271-0020N-001 | X01 |
| 38 | 37 | HW | 09/06/2011 | COMPAL | EMI issue | Add L107 & R1656,R1657 | X01 |
| 39 | 15,30 | HW | 09/06/2011 | COMPAL | Follow LL to reserve SM bus for BRCM LAN | Add QH8,RL50,RL51 | X01 |
| 40 | 36 | HW | 09/08/2011 | COMPAL | Follow Intel design guide | Change C412~C415 to 0.1uF for USB3.0 signal | X01 |
| 41 | 7 | HW | 09/08/2011 | COMPAL | Follow ESD recommand. | Reserve CC1141~CC144 for ESD | X01 |
| 42 | 14,15,40 | HW | 09/08/2011 | COMPAL | Crystal EA result | Change CH2,CH3 to 18pF Change C741,C743 to 39pF Change CH18,CH19 to 10pF Change CL5,CL6=33pF,RL22=510 ohm | X01 |

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| 43 | 29 | HW | 09/13/2011 | COMPAL | Follow IDT recomment | Swap R169~R172,C973~C976 connection | X01 |
| 44 | 42 | HW | 09/13/2011 | COMPAL | Change Q55,Q61 part for open soldering issue. | Change Q55,Q61 from DMN3030LSS-13 to AO4478L | X01 |
| 45 | 40 | HW | 10/13/2011 | COMPAL | Change board ID to X02 | Change R875 to 62Kohm | X02 |
| 46 | 42 | HW | 10/13/2011 | COMPAL | Rated Vgs of Q61 is 25V | De-pop R1627 | X02 |
| 47 | 39 | HW | 10/13/2011 | COMPAL | SMSC change 5048 pin A23 to GPIOI0 | Re-link ECE 5048 symbol | X02 |
| 48 | 40 | HW | 10/13/2011 | COMPAL | SMSC review feedback | Reserve R1658 and R1659 100Kohms to GND for I2S disabled | X02 |
| 49 | 41 | HW | 10/13/2011 | COMPAL | Change reset IC to RT9818A-44GU3 | Update U4 symbol and add R1629 for backup of inrush prevention. Change RSMRST# pull up with 100Koms. Pop R1655 and de-pop R1623.Delete R1649~R1654 | X02 |
| 50 | 39 | HW | 10/13/2011 | COMPAL | When suspend/resume cycles, wireless SW GPIO IRQs keeps giving | Change pull up rail to +3.3V_ALW for WIRELESS_ON#/OFF | X02 |
| 51 | 29 | HW | 10/13/2011 | COMPAL | 15" UMA speaker no sound issue | Pop snubber on speaker trace with C: 2200pF and R: 3.3ohms. Change bead rated current from 200mA to 2A. | X02 |
| 52 | 29 | HW | 10/13/2011 | COMPAL | EMI request | Pop C981,C982,C983,C985,C986,C987 | X02 |
| 53 | 27 | HW | 10/13/2011 | COMPAL | Depop HDD control power circuit for cost down. | Depop R1624,Q28,R500,R499,R617,C393 | X02 |
| 54 | 30 | HW | 10/18/2011 | COMPAL | Crystal EA result | Change YL1 to 3G025000FA1H, CL5,CL6 to 12pF.RL22 to 200 ohm. | X02 |
| 55 | All | HW | 10/18/2011 | COMPAL | For cost saving. | Change 0 ohm to R-short. | X02 |
| 56 | 42 | HW | 10/26/2011 | COMPAL | 1V leakage on 3.3V_RUN during system boot | Pop Q69 and R929 | X02 |
| 57 | 42 | HW | 10/26/2011 | COMPAL | Inrush current with Smart Card detect fail issue | change C763 and C766 to 2200p | X02 |
| 58 | 43 | HW | 10/27/2011 | COMPAL | LED Conn PIN definition change | JLED1 PIN define change | X02 |
| 59 | 37 | HW | 10/27/2011 | COMPAL | Remove 2pin connector for Audio performance | Remove JAG1 2 pin connector. | X02 |
| 60 | 42 | HW | 11/01/2011 | COMPAL | Change MOSFET to wihtout Schottky Diode for +1.5V_RUN leakage issue | change QC3, Q59 as AO4304L from AO4728L | X02 |
| 61 | 14 | HW | 11/15/2011 | COMPAL | RTC issue | change CH2, CH3 to 15pF | X02 |
| 62 | 14 | HW | 11/15/2011 | COMPAL | S5 power consumption over spec. | depop RH288 | X02 |

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| 63 | 34 | HW | 11/29/2011 | COMPAL | S3 had leakage in +3/5V_RUN | De-pop R725, remove R695 and add +3.3V_RUN pull high at PCH side(RH361) | X02 |
| 64 | 32 | HW | 11/29/2011 | COMPAL | TPM is changed to AT97SC3204-X2A18-AB | U39(TPM) is changed to SA00004WQ10 (AT97SC3204-X2A18-AB) for WIN8 support | X02 |
| 65 | 32 | HW | 11/29/2011 | COMPAL | +3.3V_RUN Giltch when AC plugin | Add D87, R1662 and R1663 (pull high to +3.3V_RUN_TPM) for HW solution backup | X02 |
| 66 | 14~21 | HW | 11/29/2011 | COMPAL | Change PCH to C1 version | Change UH4 to SA00005AG1L(HM77 for non vpro) | X02 |
| 67 | | HW | 11/29/2011 | COMPAL | Change RC value at Gate of MOS Load SW to modify power rail soft start timing | RC72 from 100K to 330K; RC143 form 330K to 1M; CC136 form 0.1u to 0.022u R412 from 100K to 470K; R1632 form 1M to 4.7M; C293 form 0.1u to 0.022u R507 from 100K to 470K; R517 form 1M to 4.7M; C400 form 0.1u to 0.022u R722 from 100K to 470K; R1625 form 1M to 4.7M; C644 form 4700p to 220p R729 from 100K to 470K; R1628 form 1M to 4.7M; C650 form 4700p to 220p R917 from 100K to 470K; R1617 form 1M to 4.7M; C770 form 4700p to 220p R920 from 100K to 470K; R1610 form 470K to 2.2M; C771 form 4700p to 470p R930 from 100K to 330K; R1611 form 470K to 1M; C773 form 2200p to 100p R906 from 100K to 470K; C763 form 2200p to 220p R912 from 100K to 470K; C766 form 470p to 220p | X02 |
| 68 | 36 | HW | 12/01/2011 | COMPAL | Change P/N for HF | Change C412~C415 P/N to SE076104K8L | X02 |
| 69 | 35 | HW | 12/01/2011 | COMPAL | Reserve 0.1uF CAP to GND for ESD request | reserve CE14, CE20, CE22, CC151, CC152, CC153 to GND | X02 |
| 70 | 19 | HW | 12/05/2011 | COMPAL | Change LH1 from bead to Inductor for CRT | Change LH1 to 1uH Inductor(SHI00007W0L) | X02 |
| 71 | 17,38 | HW | 12/07/2011 | COMPAL | EMI solution for E-Docking USB port | Swap USB Port7 and Port8 and reserve a choke(L108) at E-Docking side: Port7 from NA to E-docking Port8 from E-Docking to NA | X02 |
| 72 | 24,32,37 | HW | 12/07/2011 | COMPAL | Change USB9,12,13 CMC to 180ohm for EMI request | Change L10,L52,L107 to SM070002X00(OCF2012181YZF) | X02 |
| 73 | 37 | HW | 12/08/2011 | COMPAL | Follow CONN List_1130A Change JAUD1 to ACES_51522-0200N-P01 | Change JAUD1 to ACES_51522-0200N-P01 | X02 |
| 74 | 22 | HW | 12/09/2011 | COMPAL | Thermal requests to change OTP from 88 to 92 | Change R406 from 953ohm to 1.24Kohm | X02 |
| 75 | 41 | HW | 12/09/2011 | COMPAL | To prevent inrush current at reset IC input | Change R1629 from 0ohms to 33ohms resistor | X02 |
| 76 | 19 | HW | 12/09/2011 | COMPAL | For CRT issue | Change CH36 from 10uF to 22uF | X02 |
| 77 | 25 | HW | 12/13/2011 | COMPAL | Change HDMI R,C value for EMI request | Change R448,R449,R450,R452,R453,R454,R455,R456 from 680ohm to 604ohm; C1209~C1216 from 4.7pF to 3.9pF | X02 |
| 78 | 42 | HW | 12/15/2011 | COMPAL | +3.3V_SUS sequence timing | R911 from 100K to 470K; R1618 from 1M to 4.7M; C767 from 4700p to 220p | X02 |
| 79 | 43 | HW | 12/15/2011 | COMPAL | Change current limit resistors of LED | R934 from 1.2K to 820, R957 from 1.2K to 1K, R951 from 330 to 270, R949 from 1.2K to 910, | X02 |

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| 80 | 34 | HW | 01/04/2012 | COMPAL | Change RC25 value for ESD | Change RC25 from 0ohm to 1kohm(ST MEMO) | A00 |
| 81 | 40 | HW | 01/17/2012 | COMPAL | SMSC creates a new catalog part number and IC marking for the MEC5055 | Change U51 P/N to SA00003TZ2L | A00 |
| 82 | 43 | HW | 02/20/2012 | COMPAL | Change current limit resistors of LED | Change R938 to 1.1k ohm, R958 to 560 ohm, R953 to 130 ohm, R951 to 470 ohm, change R939, R959, R957, R934, R949 to 1.2k ohm | A00 |
| 83 | 38 | HW | 02/24/2012 | COMPAL | Dalmore14 UMA hang on white screen issue when attached AC+media battery after hot dock. | Change R755 from 100k ohm to 10k ohm | A00 |
| 84 | 40 | HW | 02/24/2012 | COMPAL | Change board ID to A00 | Change R875 to 33K ohm | A00 |
| 85 | 33 | HW | 02/24/2012 | COMPAL | Change SD CLK damping resistor for EMI request | Change R676 from 33 ohm to 10 ohm | A00 |
| 86 | 32 | HW | 02/24/2012 | COMPAL | Change BOM option for TPM/TCM funtion | Change C550,C551,C552,C553,R659,R660,R1662,RH311 BOM option to 5@ | A00 |
| 87 | 25 | HW | 03/03/2012 | COMPAL | SMT request to change F2 footprint | For DFX concern of F2 2nd source, SP040003H0L, change F2 footprint to F_MF-MSMF050-2 | A00 |
| 88 | 14~21, 30 | HW | 03/03/2012 | COMPAL | Change PCH P/N for X-build | UH4 is changed to SA00005AG3L | A00 |
| 89 | 14 | HW | 03/03/2012 | COMPAL | De-pop resistor on PCH JTAG for power saving | De-pop RH288, RH47, RH48 and RH49 | A00 |

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